EXPERIMENTAL AND THEORETICAL ASSESSMENT OF PBGA RELIABILITY IN CONJUNCTION WITH FIELD-USE CONDITIONS

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EXPERIMENTAL AND THEORETICAL ASSESSMENT OF PBGA RELIABILITY IN CONJUNCTION WITH FIELD-USE CONDITIONS

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LIST OF ABBREVIATIONS

ATC – Accelerated Thermal Cycling

AF - Acceleration Factor

BGA – Ball Grid Array

BT – Bismaleimide Triazine

CBGA – Ceramic Ball Grid Array

CFC - Chloroflurocarbon

CI-CGA – Ceramic Interposer Column Grid Array

CSP – Chip Scale Package

CTE – Coefficient of Thermal Expansion

DCA – Direct Chip Attach

DIP – Dual Inline Package

FC – Flip Chip

FCOB – Flip Chip On Board

FEA – Finite Element Analysis

FR4 – NEMA designation Fire Resistant 4

I/O – Input/Output

IR – Infrared

PBGA – Plastic Ball Grid Array

PPGA – Plastic Pin Grid Array

PWB – Printed Wiring Board

QFJ – Quad Flat J-Lead

QFP – Quad Flat Package

QFP – Quad Flat Pack

SBGA – Super Ball Grid Array

SMT – Surface Mount Technology

SOJ – Small Outline J-Lead

SOP – Small Outline Package

SSOP – Shrink SOP

TCP – Tape Carrier Package

TQFP – Thin QFP

TSOP – Thin SOP

W-CSP – Wafer CSP

LIST OF SYMBOLS

β_w – Shape factor in s Weibull distribution

^oC – *Centigrade*

C – Fatigue Constant

D_c = Damage due to creep

D_p = Damage due to plasticity

D_t = Total damage occurring in the solder

E – Elastic modulus

F – Cumulative failure percentile in a Weibull distribution

f_{field} – Frequency of cycling in the field,

f_{ATC} – Frequency of the qualification thermal profile,

G – *Shear modulus*

K – *Kelvin*

M – Fatigue exponent

mm – Millimeter

MPa – Megapascal

N_{field} – Fatigue life, cycles, in the field

N_{ATC} – Fatigue life, cycles, in qualification or thermal cycling

N_f – Total number of cycles to failure

N_{ff} – Failure free life of a solder ball

N^l_E – Number of cycles for linear damage mapping by energy method

N^l_S – Number of cycles for linear damage mapping by strain method

N^{nl}_E – Number of cycles for non-linear damage mapping by energy method

N^{nl}_S – Number of cycles for non-linear damage mapping by strain method

N_o – Number of cycles for crack initiation

N_p – Number of cycles for crack propagation

Q – Activation energy for creep

R – Universal gas constant

s – Internal state variable for Anand's model

s^* – Saturation value of s for Anand's model

$\hat{s}$ – Coefficient for saturation for Anand's model

s_o – Initial value of the deformation resistance for Anand's model

T – Absolute temperature, Kelvin

t – Time

T_{field} – Temperature in the field

T_{max} – Maximum temperature

$T_{max,field}$ – Maximum field temperature

$T_{max,ATC}$ – Maximum temperature during accelerated thermal cycling

T_{min} – Minimum temperature

T_{ATC} – Temperature during accelerated thermal cycling

V – Volume; element volume when used with averaging

W – Accumulated plastic work or strain energy for Akay's model; change in strain energy density for Pang's model

$\Delta\varepsilon^{in}_{acc,avg}$ = Volume averaged accumulated inelastic strain

ΔW_{acc} = Accumulated inelastic strain energy density

$\Delta W_{acc,avg}$ = Volume averaged accumulated inelastic strain energy density

$\Delta W_{acc,creep}$ = Accumulated creep strain energy density

$\Delta W_{acc,palstic}$ = Accumulated plastic strain energy density

SUMMARY

With the dramatic advances that have taken place in microelectronics over the past three decades, ball-grid array (BGA) packages are increasingly being used in microsystems applications. BGA packages with area-array configuration have several advantages: smaller footprint, faster signal transmission, testability, reworkability, handling easiness, etc. Although ceramic ball grid array (CBGA) packages have been used extensively in the microsystems industry, the use of plastic ball grid array (PBGA) packages is relatively new, especially for automotive and aerospace applications where harsh thermal conditions prevail.

This thesis work has developed an experimental and a theoretical modeling program to study the reliability of two PBGA packages. The physics-based theoretical models take into consideration the time-dependent creep behavior through power law creep and time-independent plastic behavior through multi-linear kinematic hardening. In addition, unified viscoplastic constitutive models are also taken into consideration. The models employ two damage-metrics, namely inelastic strain and inelastic strain energy density, to predict the solder joint fatigue life. The theoretical predictions have been validated through air-to-air in-house thermal cycling tests carried out between – 55 °C and 125 °C. In addition, laser-moiré interferometry has been used to determine the displacement contours in a cross-section of the package at various temperatures. These contours measured through moiré interferometry

have also been used to validate the thermally-induced displacement contours, predicted by the models. Excellent agreement is seen between the experimental data and the theoretical predictions.

In addition to life prediction, the models have been extended to map the field-use conditions with the accelerated thermal cycling conditions. Both linear and non-linear mapping techniques have been developed employing inelastic strain and strain energy density as the damage metric. It is shown through this research that the symmetric MIL-STD accelerated thermal cycles, currently in practice in industry, have to be modified to account for the higher percentage of creep deformation experienced by the solder joints in the field-use conditions. Design guidelines have been developed for such modifications in the accelerated thermal cycles.

CHAPTER I

INTRODUCTION

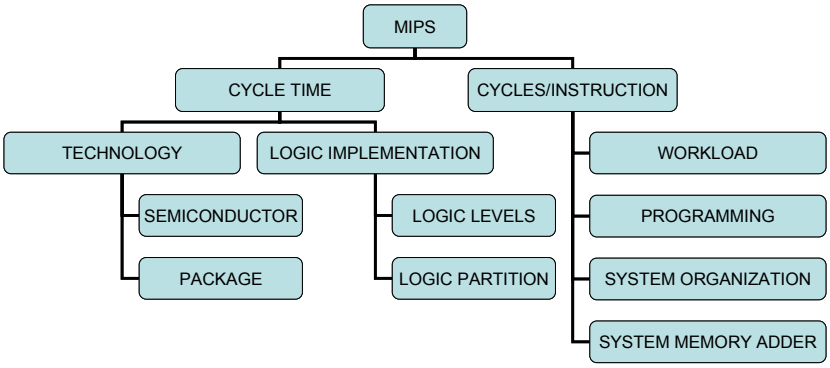
1.1 Packaging Functions and Necessity

Electronic packages contain numerous electrical components which include transistors assembled on integrated circuit (IC) chips, resistors, diodes, capacitors and other components. To form circuits, these components need to be interconnected with each other and these individual circuits in turn needed to be connected with each other to form functional entities. As the level of integration continues to increase, these intercircuit connections are steadily migrating to IC chips. IC chips and their interconnections require mechanical and environmental protection. These electrical circuits also need to be supplied with electrical power which is consumed and converted into thermal energy. For optimal performance, these circuits need to be maintained within certain temperature range. Thus packaging has four main functions:

- Signal distribution
- Power distribution
- Heat dissipation (cooling)
- Mechanical, chemical and electromagnetic protection of components and interconnections

Figure 1.1 shows the factors affecting the performance in Million Instructions per Second (MIPS) of a high performance computer system. It can be seen that

packaging plays an important role in determining the speed with which the computer operates.



$$Performance\ (MIPS) = \frac{1000}{cycle\ time\ X\ cycles\ \ per\ instruction}$$

Figure 1.1 Factors affecting the performance of a computer system

Over the past few years, the on-chip delay in IC semiconductor devices has been reduced rapidly. However, the signal delay in package ICs was not able to be reduced as much as that of the on-chip ICs. Thus, packages have become a bottleneck of a computer system [Lau and Erasmus, 1993]. It can also be seen from Figure 1.2 that a 50% improvement in logic performance for a computing system results in less than 23% overall gain if the packaging does not change. Ensuring the optimal design of an electronic package is hence of utmost importance.

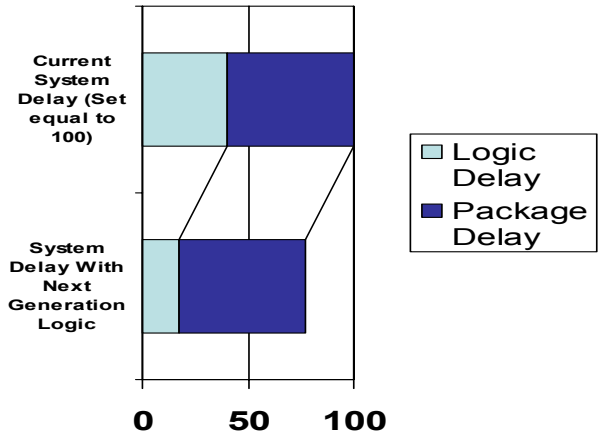
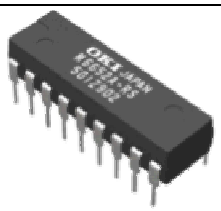
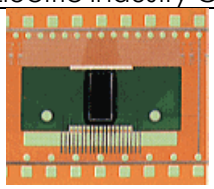
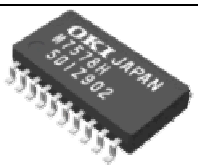
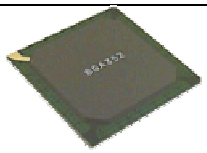
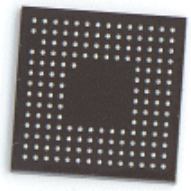


Figure 1.2 Logic and package delay [Tummala. et al., 1997]

1.2 Packaging Evolution

The past few decades have seen gradual evolution in packaging technology to keep up with the increasing demand for faster signal speed, higher Input/output (I/O) connection per chip, higher I/O density, lower weight and lower cost. Table 1.1 shows the various packaging technologies that are in use today. The packaging technologies in 1970s were mainly through-hole Dual In-Line Packages (DIPs). In DIPs, the I/Os are in the form of pins and are distributed along the sides of the package. To achieve higher I/O connections, the Pin Grid Array (PGA) packages were introduced wherein the I/Os are distributed in an area array fashion. The small outline packages were then introduced for low I/O memory applications because of the cost benefits it offered. The Quad Flat Package (QFP) was developed as an extension of the small outline package. QFPs have higher I/O connections compared to small outline packages.

Table 1.1 Packaging technologies [Oki Electric Industry Co. Ltd., 1997-2002]

	DIP Dual In-Line Package		TCP Tape Carrier Package
	SOP Small Outline Package		QFJ Quad Flat J-Lead
	SOJ Small Outline J-Lead		QFP Quad Flat Pack
	SSOP Shrink Small Outline Package		TQFP Thin Quad Flat Pack
	TSOP Thin Small Outline Package		BGA Ball Grid Array
	W-CSP Wafer-Level Chip Scale Package		PPGA Plastic Pin Grid Array

The through-hole packages mentioned above consume a significant amount of Printed Wiring Board (PWB) area. As an enhancement to these through-hole packages, in the late 1980s, surface mount packages with solder balls were developed as an alternative. Surface mount packages significantly increase the I/O count of the packages as compared to their through-hole counterparts. Ball Grid Packages (BGA) packages are an example of this technology. These packages are smaller, thinner, lighter and provide higher

signal speed due to the short interconnect length of the solder ball. Figure 1.3 shows the evolution of packaging technology over the last three decades.

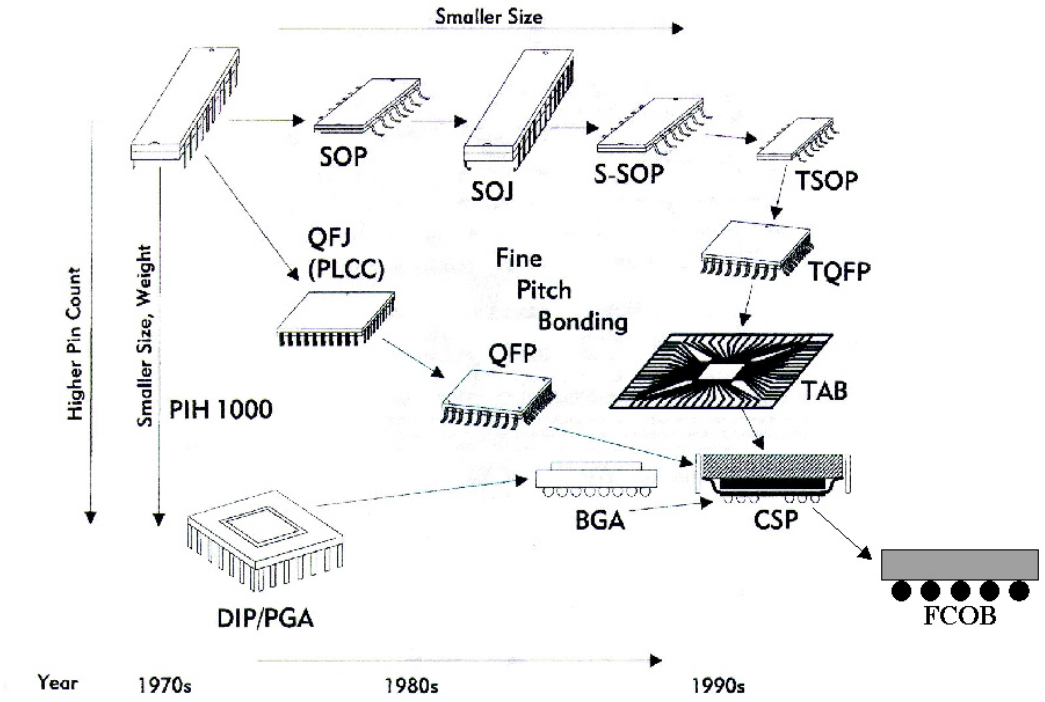


Figure 1.3 Evolution of electronic packaging technology [Tummala et al, 1996]

Chip Scale Packages (CSP) developed during the late 1990s and they meet most of the demands of the modern electronics. The packaging technology has come a long way from being around 100 times the size of the die in the 1970s to about 1.2 times the size of the die at the present age.

1.3 Plastic Ball Grid Array Package

The Plastic Ball Grid Array (PBGA) packages were developed due to the combined efforts of Motorola and Citizen where they replaced the ceramic substrate of the Ceramic BGA package by Bismaleimide Triazine (BT) substrate and included a plastic molding process for the chip and the substrate [Freyman and Pennisi, May 1991]. Figure 1.4 shows the schematic of the cross section of a

PBGA package. It consists of a silicon IC, gold wires and bonds, die attach, copper pads, molding compound, BT epoxy substrate, solder balls, vias for ground/signal/thermal, plated copper conductors and a solder mask.

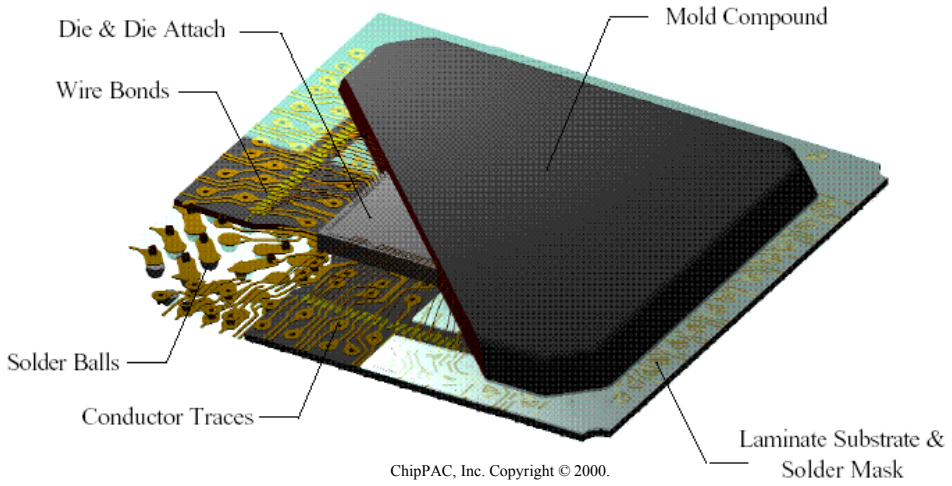


Figure 1.4 PBGA package [ChipPAC Incorporated, 2000]

The overmold protects the silicon IC from moisture, ionic contaminants and from hostile operating environments such as mechanical shock and vibration. PBGAs are typically used for Static Random Access Memory (SRAM) with high speed applications. It is also used for Application Specific Integrated Circuits (ASICs) and microprocessors with less than 600 I/O count and with less than 75 MHz clock frequencies [Lau, 1995].

PBGAs offer significant surface mounting advantages over conventional leaded plastic packages. A primary reason being that the defect levels during solder joint attachment is extremely low. IBM recently reported defect levels of less than 1 ppm on a per-joint basis for PBGA package as against to about 20 to 100 ppm for a QFP package [Derman, 1994]. The placement tolerances for the PBGA package are not as critical as it is for the plastic QFP package because of

the large pad pitch and self-aligning ability. The self-aligning ability is due to capillary action and surface tension forces acting to align the package to solder lands on the motherboard. Because of this self-aligning property, the package solder balls can be misaligned up to 40 percent relative to the board pads and the package will still align itself during reflow. PBGA package hence offers a low cost solution for high yield, light weight and high performance package.

1.4 Super Ball Grid Array Package

Super Ball Grid Array (SGBA) packages are a modified version of PBGA package. It was developed by Amkor for high-performance applications requiring stringent thermal and electrical requirements. A schematic of the SBGA package is shown in Figure 1.5. SBGA package is a cavity down package where the chip is inverted and faces downwards. Interconnections from the periphery of the chip are routed using gold wire bonds. The silicon IC and the gold wire bonds are protected by an encapsulant made of epoxy. A copper heat spreader layer fully covers the top of the package and it serves to increase the heat dissipation. The heat spreader also serves to protect the silicon IC from harmful electromagnetic radiation.

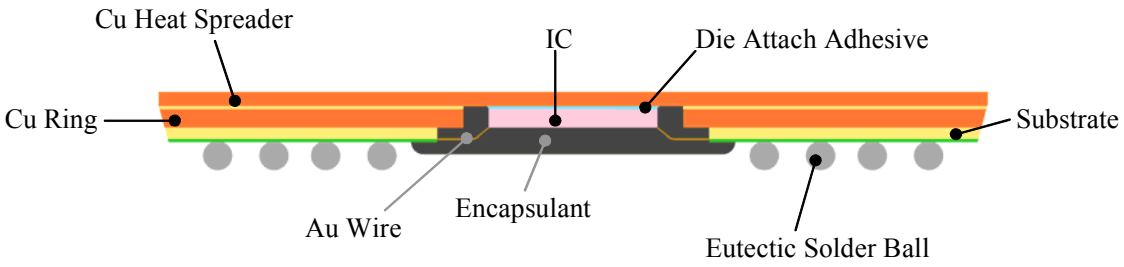


Figure 1.5 SBGA package

1.5 Qualification of BGA packages

BGA packages are used typically for both military and consumer end applications. Qualification of these packages for its reliability involves subjecting them to Accelerated Thermal Cycling (ATC). The temperature range, time of dwell and ramp rate are the three important parameters representing any ATC. These parameters should be based on the type of application the package is intended for [Syed and Doty, 1999]. However, in the absence of specific guidelines, the industrial practice is to subject the devices to standard legacy qualification cycles without ample consideration for the application of the product. If the qualification is excessive, the packages may be over-designed and thus the design may be too costly and may sacrifice the electrical and thermal performance for reliability. Hence, a physics-based mapping methodology that maps the solder degradation or damage under field-use conditions with the solder degradation or damage under ATC is necessary.

During thermal excursions, solder undergoes both time-independent plastic deformation and time-dependent creep deformation. The plastic deformation is due to dislocation movement under the influence of shear stresses leading to slip bands, whereas the creep is due to diffusional flow of vacancies leading to change in the shape of the grains. Hence, the two mechanisms that accelerate and fatigue failure are fundamentally different. Therefore, it is necessary to ensure that the packages subjected to ATC experience equivalent proportion and magnitudes of creep and plastic deformation, as they would experience during their entire field use. Any thermal cycling regime that introduces different proportion of plastic and creep strain or strain energy

compared to the field-use conditions may not be suitable to qualify packages for that application. For example, packages that are used in harsh conditions with an intended life of over 10 years, as in automotive and aerospace applications, are likely to experience considerable amount of creep damage due to large amount of temperature dwell inherent under such conditions [Pucha et al, 2001]. On the other hand, packages that are used in applications with frequent on and off and with short operational life (such as cell phones, laptops) are likely to experience considerable amount of dislocation-induced damage. Therefore, the number of thermal cycles, the temperature range, and the dwell times should be carefully tailored depending on the intended use of the electronic package.

1.6 Outline of the Thesis

Chapter II presents the literature review relevant to this work. Chapter III discusses the objectives of the present research and the approach followed. Chapter IV deals with the virtual reliability assessment of Plastic Ball Grid Array (PBGA) packages. Chapter V deals with the experimental validation of PBGA packages. Chapter VI deals with the virtual reliability assessment of Super Ball Grid Array (SBGA) packages. Chapter VII deals with the experimental validation of SBGA packages. In Chapter VIII, the field-use correlation and the damage mapping methodologies will be discussed. Chapter IX provides conclusions and summarizes the work.

CHAPTER II

LITERATURE REVIEW

The present work involves developing an experimental and theoretical modeling program to study the reliability of two Plastic Ball Grid Array packages. The models developed have been validated experimentally and have been used for prediction of the fatigue life of the solder joint. In addition, the models have been extended to map the field-use conditions with the accelerated thermal cycling conditions. The present chapter, therefore, reviews the literature in the following areas.

- Build and test approach vs. virtual reliability approach
- Reliability studies on Ball Grid Array packages
- Solder material models
- Fatigue models
- Model validation methodologies
- Qualification and mapping

2.1 Introduction

Electronic packages are used in diverse field-use conditions. There is therefore no unique method that can be adopted to qualify these packages. Figure 2.1 shows the different ATC regimes used by the industry to qualify a package. In the absence of any specific qualification guidelines the industry practice is to subject the package to legacy ATC without due consideration to

the actual type of failure mechanism occurring in the package during its field-use. For the most part, these standard ATCs are either Military standard (MIL-STD) based or acceleration factor based and hence fail to take into consideration the actual physics behind the failure occurring in the package.

The military standard qualification tests are excessive for packages that are not used in harsh environment. Moreover, when the packages are subjected to temperatures that they are not likely to experience in the field, the failure modes seen during qualification tests can be different than the failure modes seen during field-use. Hence, the number of accelerated thermal cycles, the temperature range and the time of dwell used for qualifying a microelectronic package should be based on the type of application the package is intended for. The accelerated thermal cycles should accelerate the failure mechanism and not alter it.

Acceleration factor approach uses an industry standard thumb-rule to assess the number of cycles needed to qualify a package during ATC. Acceleration Factor (AF) is defined as a ratio between the number of field-use thermal cycles that the package is designed for to the number of ATCs required to meet the design life.

Table 2.1 Qualification guidelines for commercial applications. TC=Thermal Cycling, AATS=Air to Air Thermal Shock, NA=Not Available [Syed and Doty, 1999]

Application	Company	Temperature Cycle	Specified Duration (Cycles)	Test Method
Consumer	A	0 to 100 C	500	TC
	B	-25 to 125 C	1000	TC
	C	-25 to 125 C	1500	TC
	D*	-25 to 125 C	600	NA
	E*	-40 to 80 C	700	NA
Cell Phone PDA PHS DVC & Other	A*	-25 to 125 C	250	N/A
	B	-40 to 100 C	800	TC
	C	-40 to 100C	800	AATS
	D*	-40 to 125 C	500	NA
	E*	-40 to 125 C	500	NA
	F*	-40 to 85 C	500	NA
	G*	-40 to 85 C	300	NA
	H*	-40 to 85 C	500	NA
	I*	-55 to 125 C	300	NA
	J*	-40 to 125 C	1000	NA
	K	-55 to 125 C	500	AATS
	L*	-65 to 125 C	350	NA
Desktop Laptop Workstation Server Disk Drives SRAM DRAM PC Card	A	0 to 100 C	1000	TC
	B	0 to 100 C	1200	TC
	C	0 to 70 C	1000	TC
	D	-25 to 100 C	1000	AATS
	E	-40 to 85 C	1000	TC
	F	-55 to 125 C	1500	AATS
	G	0 to 100 C	3000	TC
	H*	-30 to 100 C	600	NA
	I*	-40 to 85 C	800	NA
	J	-65 to 125 C	1000	TC
	K*	-40 to 100 C	800	NA
	L*	-65 to 150 C	500	NA
	M*	-30 to 80 C	1000	NA
Telecomm	A	0 to 100 C	3000	TC
	B	0 to 100 C	1500	TC

* source: Kyocera

The acceleration factor for tin-lead near eutectic solder is given by equation 2.1 [Norris and Landzberg, 1969].

$$AF = \left(\frac{f_{field}}{f_{ATC}}\right)^{1/3}\left(\frac{\Delta T_{ATC}}{\Delta T_{field}}\right)^{2}\exp\left[1414\cdot\left(\frac{1}{T_{\max,field}}-\frac{1}{T_{\max,ATC}}\right)\right] \qquad \text{Eq (2.1)}$$

where f_{field} is the frequency of temperature cycling observed during field-use, f_{ATC} is the frequency of thermal cycling during ATC, ΔT_{ATC} is the maximum temperature range during ATC, ΔT_{field} is the maximum temperature range during field-use, $T_{max,field}$ is the maximum field-use temperature, and $T_{max,ATC}$ is the maximum temperature during ATC.

Equation 2.1 was developed by modifying the coffin-manson equation by a frequency term [Norris and Landzberg, 1969] and by an Arrhenius-type term [Lin et al, 1970]. If the solder failures do not follow the Arrhenius modified coffin-manson equation, then acceleration factor equation cannot be used with enough confidence. Equation 2.1 does not take the assembly process and the type of package into consideration. A virtual reliability model that takes into account the actual physics-of-failure would hence be necessary.

2.2 Virtual Reliability Models

Figure 2.1 shows a schematic of the basic idea behind virtual reliability modeling methodology. A reliability assessment numerical model is first built that takes into account the actual geometry details of the package. The material properties of the commonly used materials like copper, BT, FR4, silicon and eutectic solder can be obtained from the widely available material database or from the literature. For newly developed polymeric materials and lead-free solders however, material characterization should be performed to obtain their linear and non-linear properties.

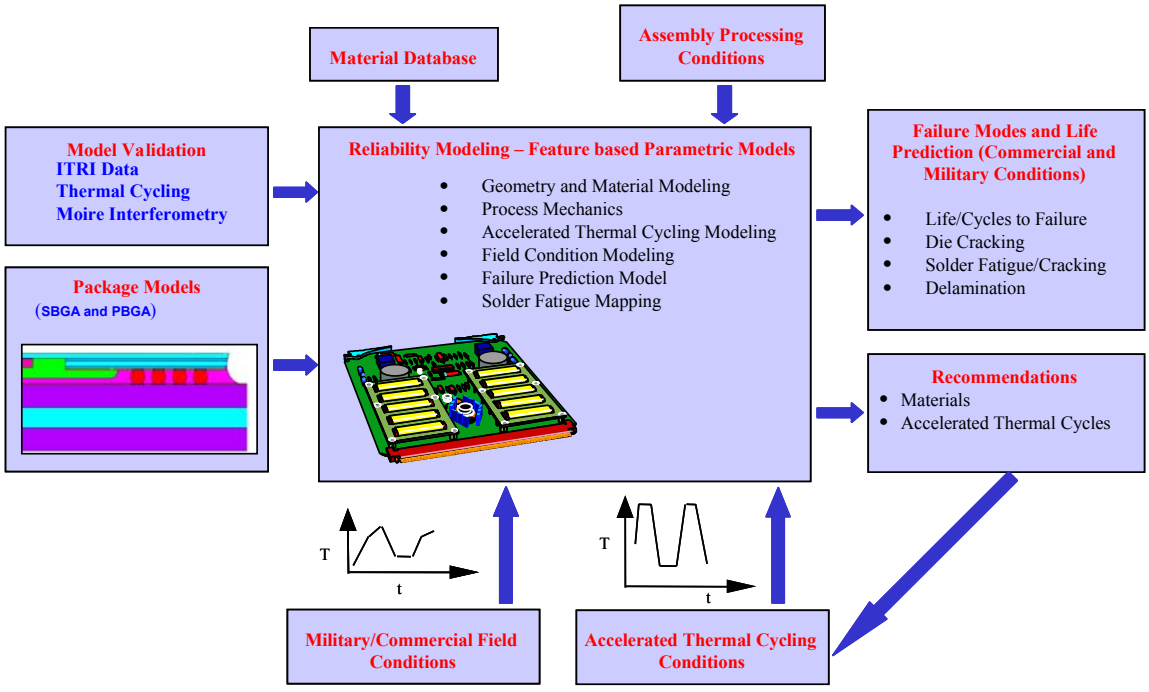


Figure 2.1 Schematic of virtual reliability methodology

The actual assembly process of the package can also be taken into consideration to assess the residual stress and strains present in the package after its fabrication. These stresses and strains can then be factored in while determining the fatigue behavior during field-use and ATC. Virtual modeling methodology however, needs to be validated experimentally to ensure the accuracy of the obtained results. Virtual modeling through numerical analysis can help us to obtain failure modes like die-cracking, solder joint fatigue behavior, delamination etc. Based on the results obtained, appropriate design recommendation can be made to ensure the mechanical reliability of the package.

2.3 Fabrication process for a PBGA Package

The equipment used to manufacture PBGA package is similar to the ones used for QFP package. Hence, bringing about a transition from QFP to PBGA did not require investing a lot of money on the equipment. Assembly processes such as chip attachment, wire bonding and molding can be done using conventional automated plastic IC assembly equipment but with few modifications to fixtures, temperatures and materials.

Figure 2.2 shows a schematic of the cross-section of a typical PBGA package. PBGA packages generally use an organic BT laminate as the substrate with two or more metal layers (typically copper) formed on substrate. The PBGA substrates are punched from a bigger PCB board and each site is electrically tested and visually inspected. The punched strips are then packed and shipped to the IC assembly site.

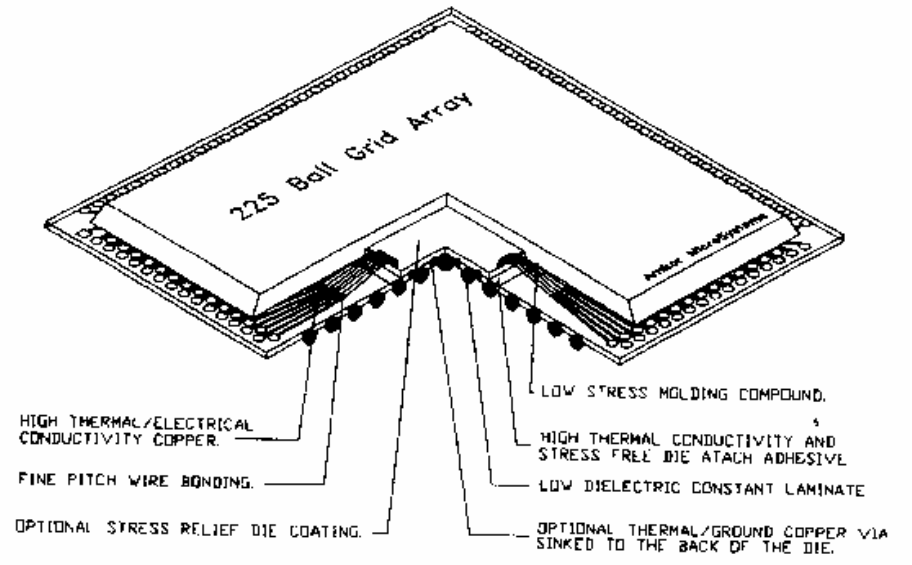


Figure 2.2 Cross-section of a PBGA package [Lau, 1995]

At the IC assembly site, the IC wafers are diced into individual chips using a high-speed diamond-impregnated cutting blades. These chips are then mounted to the sites on the PBGA strip using silver-filled epoxy. The epoxy material is then cured at about 175°C for one hour in an air-circulating oven.

The I/O's at the periphery of the chips are then thermosonically wire-bonded using gold bonding wires to the I/O pads on the PBGA strip. The bond pad metallurgy on the PCB is typically copper-nickel-gold. The wire bonded strips are then transfer-molded with an epoxy mold compound and cured in an air-circulating oven, typically for 6 hours at 175°C. Marking is performed on the molded surface using either UV curable ink or laser marking.

The next step is to attach solder balls to the pads on the bottom side of the substrate. Flux is applied to the balls and solder material is placed on the pads. The whole package is then reflowed in an Infra Red (IR) furnace to form metallurgical solder joints. The units are cleaned in a CFC-free process to remove any remaining residues of the solder flux material. These units are punched out from the strips and are ready to use.

2.4 Assembly of a PBGA Package

Assembly of a PBGA package involves mounting the package on the motherboard. The first step in the process is to screen print the solder paste onto the pads on the motherboard. Typical solder pastes used for a PBGA package are 63Sn/37Pb, 60Sn/40Pb and 62Sn/36Pb/2Ag. PBGA packages are known to be insensitive to the thickness of the solder paste that is screen printed.[Lau, 1995]. Hence, the thickness of the screened paste is generally

governed by the other components present on the motherboard. Thicknesses ranging from 0.1 mm to 0.2 mm are typical.

PBGA packages are picked from tape reels or trays and placed on the screen printed solder paste using either mechanical centering or package edge recognition technique. The whole assembly is then reflowed either in an IR oven or in a hot-air convection furnace with nitrogen. After reflow, the assembly is then cleaned using a CFC-free (Cloroflurocarbon free) cleaning process. The high surface tension of the solder joints permits placement of the package on both sides of the motherboard during subsequent reflow processes. Once the assembly parameters are established for a particular configuration, the process control involves monitoring the solder ball attach process with electrical test yields.

2.5 Surface Evolver

Surface evolver is a software program that is used to determine the shape of the solder ball after the reflow process. The program was developed at the University of Minnesota due to the efforts by Brakke (1992). The surface evolver works by minimizing the energy of the surface. The energy of the surface can be due to surface tension and gravity. The surface evolver allows the use of constraints on the surface whose energy is to be minimized. The minimization of the surface energy is achieved by using the process of evolution by mean curvature [Brakke, 1977].

The energy present in a solder ball is mainly due to the presence of surface tension and gravitation. A three dimensional solder ball is represented by

a two dimensional surface. Finite-element method is used which permits representation of the surface using vertices, edges and facets. This surface is then subjected to geometrical constraints that the solder joints would experience during the reflow process. The standoff height of the solder joint and the actual volume of the solder material are the two necessary constraints. The standoff height of the solder joint can be found by cross-sectioning the package after its assembly. During situations wherein the cross-sectioning cannot be done, the software permits the use of the vertical force acting on the solder joint to be used instead of the standoff height. The actual volume of the solder material can be estimated based on the dimension of the stencil used for screen printing. PBGA and SBGA packages are normally shipped with pre-bumped solder pads. The volume of these pre-bumped solder balls should be added to the volume of the screen printed solder ball to get the final volume of the solder joint after reflow process. If *d* represents the diameter of the hole in the stencil through which the solder balls are screen printed and if *t* represents the thickness of the stencil used for screen printing, the total volume of the solder ball is then given by Equation 2.2.

$$Total\ Volume = Volume\ of\ the\ bumped\ solder\ ball + \frac{1}{4}\pi d^2 t \qquad \text{Eq. (2.2)}$$

Figure 2.3 shows a typical evolution process of the solder ball geometry. The final geometry of the solder ball can be exported directly to FEA software like ANSYS.

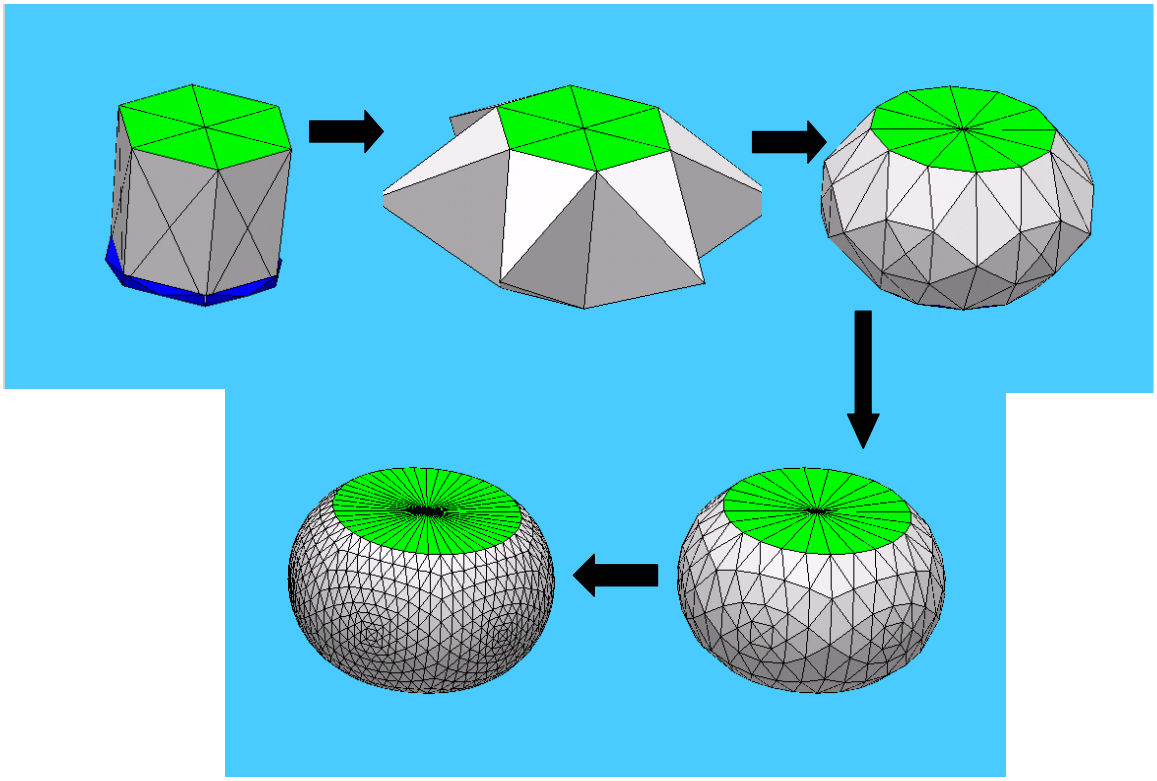


Figure 2.3 Evolution process of a solder ball using surface evolver

2.6 Constitutive Modeling for the Solder Material

Eutectic Pb-Sn solder material has a homologous temperature of over 0.5 even at room temperature. This would mean that the solder would exhibit creep even at room temperature. Material modeling should hence include this rate-dependent deformation behavior either in the form of an explicit creep equation or in the form of unified viscoplastic model [McDowell et al, 1994, Anand, 1985]. The creep in solder can be represented either in the power law form [Ju et al, 1994] or the hyperbolic sine form [Garafalo, 1965]. Using either one of these would also require us to include rate-independent plasticity in the material modeling. Unified viscoplastic models however, does not separate the deformation mechanism into creep and plasticity. Both of them are combined into a rate-dependent form and used while modeling the behavior of the solder.

The following sections illustrate the constitutive models that were used in the present work.

2.6.1 *Rate-Independent Plasticity*

The rate-independent deformation behavior of the solder material can be represented by the power law form as shown in equation 2.3.

$$\gamma_p = C_2\left(\frac{\tau}{G(T)}\right)^m \qquad \text{Eq (2.3)}$$

where, γ_p is the shear strain, C_2 and m are experimentally determined constants, τ is the shear stress, and $G(T)$ is an empirically derived expression for the shear modulus and is given by equation 2.4.

$$G = G_0 - G_1 T' \qquad \text{Eq (2.4)}$$

where, G_0 and G_1 are experimentally determined constants, and T' is in °C. Constants for the 62Sn/36Pb/2Ag solder has been reported before [Darveaux et al 1992].

2.6.2 *Power- Law Creep*

Power-law creep that has been reported for eutectic and near-eutectic solder [Ju et al 1994] represents the climb-controlled deformation region. The form of power law creep is shown in equation 2.5.

$$\dot{\varepsilon}_c = A\sigma^n e^{-(Q/RT)} \qquad \text{Eq (2.5)}$$

Here, $\dot{\varepsilon}_c$ represents the steady state creep strain rate, A and n are experimentally determined material constants, σ is the current stress, Q is the

activation energy for creep, *R* is the universal gas constant, and *T* is the temperature in the Kelvin scale.

2.6.3 *Garafalo Creep (Hyperbolic Sine creep)*

Garafalo creep is used for higher stress region where the power law behavior breaks down. The general form of the Garafalo creep equation that has been reported for 62Sn/36Pb/2Ag [Darveaux et al] is shown in equation 2.6.

$$\dot{\gamma}_s = C_1 \frac{G}{T}\left[\sinh\left(\alpha\frac{\tau}{G}\right)\right]^n \cdot \exp\left(\frac{-Q}{kT}\right) \qquad \text{Eq (2.6)}$$

where $\dot{\gamma}_s$ is the steady state shear strain rate, C_1, n, and α are experimentally determined material dependent constants, Q is the material activation energy for creep, τ is the shear stress, G is the shear modulus, *T* is the absolute temperature, and *k* is Boltzmann's constant.

2.6.4 *Unified Plasticity Model (Anand Model)*

Various viscoplastic models have been formulated by many researchers [McDowell et al, 1994, 1985]. Unified viscoplastic model uses internal state variables to represent the deformation behavior of the material under fatigue loading. This work uses the Anand's viscoplastic model which uses a single internal state variable (ISV) '*s*' which measures the isotropic resistance offered by the solder to the plastic flow. This model can also be easily implemented in the commercially available Finite Element software like ANSYS. Anand's model was originally developed for hot working process rather than for the thermal cyclic loading. Moreover, isothermal fatigue experiments conducted on solder material revealed that solders exhibit Bauschinger effect [Busso and Kitano, 1994] which

leads to kinematic hardening during fatigue. Modeling this behavior would require additional internal state variables apart from 's'. However, the importance of Bauschinger effect is somewhat reduced at higher homologous temperatures and relatively low strain rate regimes that the solder material experiences [Wang et al, 2001]. It has also been shown that Anand's model offers reasonably close results when compared to a combination of plasticity and creep model [Tunga et al, 2002].

Two basic features of Anand's model are that this model needs no explicit yield criterion and assumes no loading/unloading criterion. The plastic strain is assumed to take place at all nonzero stress values. A single scalar ISV 's' is used to represent the isotropic resistance to plastic flow offered by the material. This ISV has the dimension of stress and is called as deformation resistance. Anand's model can represent the strain rate and temperature sensitivity, strain rate history effects, strain hardening and the restoration process of dynamic recovery. The ISV 's' represents an averaged isotropic resistance to macroscopic plastic flow offered by the isotropic strengthening mechanisms such as dislocation density, solid solution strengthening, grain effects etc. Equation 2.7 shows the functional form of the flow equation that accommodates the strain rate dependence on the stress.

$$\dot{\varepsilon}_p = Ae^{(-Q/RT)}\left[\sinh\left(\xi\frac{\sigma}{s}\right)\right]^{1/m} \qquad \text{Eq (2.7)}$$

where, $\dot{\varepsilon}_p$ is the inelastic strain rate, *A* is the pre-exponential factor, *Q* is the activation energy, *m* is the strain rate sensitivity, *ξ* is the multiplier of stress, *R* is the gas constant and *T* is the absolute temperature. The ISV enters the flow

equation only as a ratio with the equivalent stress. The temperature dependency is incorporated via a classical Arrhenius term. The stress and strain rate dependency however is of the Garafalo form which was discussed before. The evolution of the ISV 's' is given by the equations 2.8 and 2.9.

$$\dot{s} = \left\{ h_o \left| 1 - \frac{s}{s^*} \right|^a \cdot sign\left(1 - \frac{s}{s^*} \right) \right\} \cdot \dot{\varepsilon}_p ; a > 1 \qquad \text{Eq (2.8)}$$

$$s^* = \hat{s} \left[\frac{\dot{\varepsilon}_p}{A} e^{(Q/RT)} \right]^n \qquad \text{Eq (2.9)}$$

where, h_o is the hardening/softening constant, a is the strain rate sensitivity of hardening/softening. The quantity s^* represents a saturation value of s associated with a set of given temperature and strain rate as shown in equation 2.9. $\hat{s}$ is a coefficient of saturation, and n is the strain rate sensitivity for the saturation value of deformation resistance.

As seen from the model, we need to determine nine material constants to be able to model the material behavior adequately. They are: A, Q, ξ, m, h_o, $\hat{s}$, n, a, plus the initial value of the deformation resistance, s_o.

2.7 Fatigue Modeling of Solder Joints

Fatigue models are used to determine the number of cycles that the package survives before failure occurs. The low cycle fatigue behavior of solder joints is of great significance to the electronic packaging community because of the complicated multiaxial loading that it undergoes during its operation. It is imperative that we understand the kind of loading the solder experiences when used in electronic systems. The loading that solder experiences is thermo-

mechanical and multiaxial in nature. Depending on the application, the temperatures the solder experiences can be as low as -40°C to as high as 125°C. The size of the material is considerably small (typically < 3mm) compared to the bulk specimens that are used for fatigue testing. Ball grid array packages typically have an encapsulant (underfill) between the substrate and the package. This serves to couple the package to the board and reduce the solder joint fatigue. Encapsulants also serve to protect the solder against moisture condensation, shock and vibration. Failure to use an encapsulant might result in degradation of the solder material due to corrosion. The ideal model should be able to take all these factors into consideration. But because of the diverse variety of packing technology that are in use today coupled with diverse field-use conditions that the solder joints experiences, it is not possible to have an unique fatigue model that would satisfy our requirement. As a result, we have numerous fatigue equations that are available for use. Most of these equations are of Coffin-Manson type equations. Some of them incorporate frequency and temperature effects [Engelmaier, 1983, Shi et al, 1999] to ensure that the fatigue model is applicable to a reasonably wide range of package configurations. The following sections review four different fatigue models that were used in this work.

2.7.1 Darveaux Model

Darveaux model is an energy based model and uses accumulated plastic energy density as a damage metric to find the number of cycles to failure. The accumulated plastic energy deinsity can be found by Finite Element Analysis (FEA) and is given by equation 2.10 [ANSYS Inc, 1994].

$$\Delta W_{acc} = \sum_{i=1}^{NINT} \sum_{j=1}^{NCS} \{\sigma\}^T \{\Delta\varepsilon^{pl}\} vol_i \qquad \text{Eq (2.10)}$$

Where, *NINT* is the plastic strain increment, *NCS* is the total number of converged substeps, σ is the current stress, $\Delta\varepsilon^{pl}$ is the plastic strain increment and vol_i is the volume of the element. The plasticity mentioned in the above equation includes rate-dependent effects. If a combination of plasticity and creep models are used in the FEA, then the plastic strain and creep strain should be combined before using in equation 2.10. Under such case the damage metric will be regarded as accumulated inelastic energy density.

Darveaux performed thermal cycling experiments on several PBGA and CBGA samples with temperatures varying from -55°C to 125°C [Darveaux, 2000]. At regular intervals few samples were pried off and the dye-n-pry technique was used to measure crack length in the solder ball during thermal cycling. It was observed that the crack growth rate remains essentially constant during thermal cycling. The number of cycles for crack initiation was determined by extrapolation. Finite Element models were built and the volume averaged plastic energy density accumulated during one thermal cycle was output as a damage metric. The volume averaged accumulated plastic energy density is given by equation 2.11.

$$\Delta W_{acc,avg} = \frac{\sum_{element} \Delta W_{acc} \cdot V}{\sum_{element} V} \qquad \text{Eq (2.11)}$$

Where *V* is the volume of a single element. Volume averaging methods have been adopted by many authors [Darveaux, 2000, Syed, 1996] to mitigate the singularity effects observed at the edge of the solder ball. This volume averaged damage metric got from FEA was then used to correlate the number of cycles for crack initiation and crack growth rate got from experiments according to equation 2.12 and 2.13.

$$N_o = K_1 \Delta W_{ave,acc}^{K_2} \qquad \text{Eq (2.12)}$$

$$\frac{da}{dN} = K_3 \Delta W_{ave,acc}^{K_4} \qquad \text{Eq (2.13)}$$

Where, K_1, K_2, K_3, and K_4 are the constants which depends on the FEA mesh used in the simulation, *a* is the crack length and $\Delta W_{ave,acc}$ is the average accumulated plastic energy density. The constants can be found from Darveaux [2000]. For the crack growing throughout the length of the solder, the number of cycles for crack propagation can be obtained using equation 2.13 along with the radius *R* of the solder ball as shown in equation 2.14a.

$$\int_0^{2R} da = \int_0^{N_p} K_3 \Delta W^{K_4} dN \qquad \text{Ea(2.14a)}$$

For many plastic and ceramic ball grid array packages, the crack growth rate was found to be fairly constant [Darveaux, 1997]. During such cases, the number of cycles for crack propagation can be reduced to the form shown in equation 2.14b.

$$N_p = \frac{2R}{da/dN} \qquad \text{Eq (2.14b)}$$

The total number of cycles to failure is then given by equation 2.15.

$$N_f = N_o + N_p \qquad \text{Eq (2.15)}$$

It should be pointed out that the crack rate data reported by Darveaux are the characteristic (63.2 percentile) data as calculated by a 3-parameter Weibull analysis. So the quantity N_f represented by equation 2.15 is actually the mean number of cycles for failure. Assuming the failure follows the Weibull distribution, the number of cycles for failure other than 63.2% can be obtained by equation 2.16 [Darveaux, 2000].

$$N = N_{ff} + (N_f - N_{ff})(-\ln(1-F))^{\frac{1}{\beta_w}} \qquad \text{Eq (2.16)}$$

Where, N_{ff} is the failure free life, F is the cumulative failure percentile and β is the shape factor for the Weibull distribution. For PBGA packages, the failure free life has been experimentally shown to be equal to approximately half the mean life of the package [Lau, 1995].

2.7.2 Pang Model

Pang's model [Shi et al, 2000] is a strain based model and uses the plastic strain range as a damage metric to find the number of cycles to failure. The form of the fatigue equation is given in equation 2.17 where, m and C are numerical constants.

$$N_f{}^m \Delta\varepsilon_p = C \qquad \text{Eq (2.17)}$$

The constants m and C were found by performing isothermal fatigue test on a solder sample at 1 Hz with the temperature varying from -40°C to 150°C. m was also found by a separate plastic flow law and its value was found to match

with the value of *m* found by isothermal fatigue experiments. The variation of *m* and C with temperature is shown in Figure 2.4.

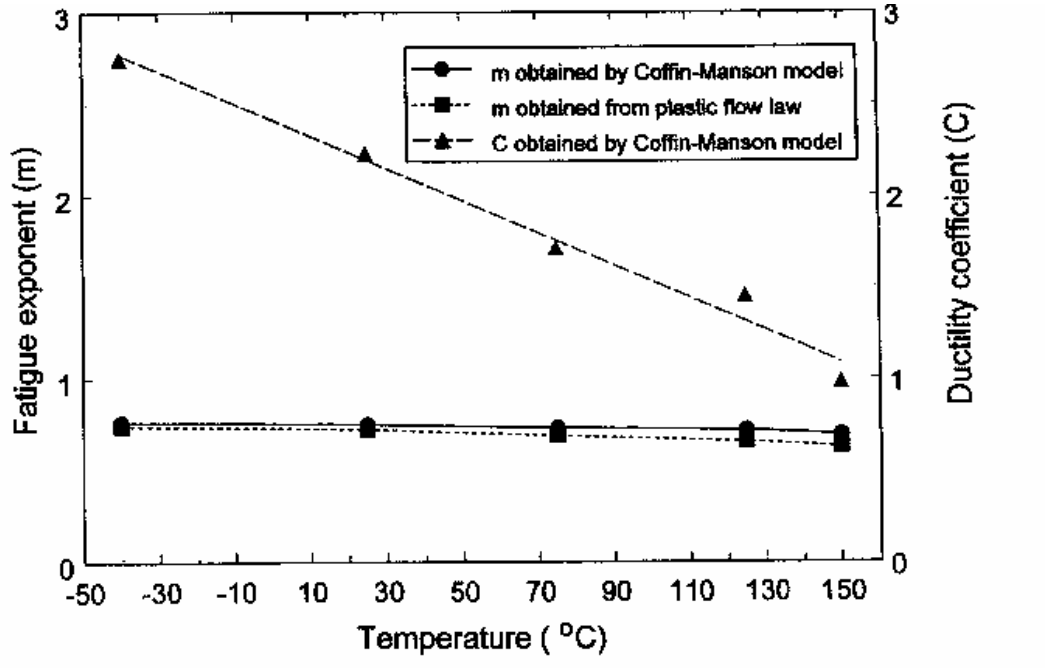


Figure 2.4 Variation of *m* and C with temperature

2.7.3 Knecht and Fox model

The Knecht and Fox [Knecht and Fox, 1991] model is a strain based model and uses the creep shear strain range as a damage metric to determine the number of cycles to failure. The fatigue life is given by equation 2.18. Where C is an experimentally determined constant and is equal to 8.9 for near eutectic solder joints,

$$N_f = \frac{C}{\Delta\gamma_{cr}} \qquad \text{Eq (2.18)}$$

The creep failure indicator data that was developed earlier [Shine and Fox, 1987], was extended to multiaxial case and the constants were found. A butt joint surface mount configuration was tested in simple mechanical loading

and was also analyzed by FEA. Good correlation with observed solder fatigue failures was observed.

2.7.4 Pan Model

Pan's model [Pan, 1994] is an energy based model and uses plastic and creep accumulated strain energy densities as damage metrics. The temperature range, ramp rate and hold time during thermal loading were taken into consideration through numerical simulations. The results from numerical simulations were used in conjunction with the experimental results from Hall and Sherry (1986) to determine the constants for the fatigue model. Equation 2.19 relates the fatigue life to the damage metrics mentioned above.

$$N_f = \frac{C}{(a\Delta W_{acc,creep} + b\Delta W_{acc,plastic})} \qquad \text{Eq (2.19)}$$

The values of the constants are shown in Table 2.2.

Table 2.2. Constants for Pan's model

Constant	**Value**
C	4550 N/mm^2
a	0.13
b	1

2.8 Model Validation Methodologies

Reliability assessment using numerical analysis involves building a model with many different materials. Naturally, the results obtained depend on the material properties used while performing the analysis. Also, the results obtained depend on the mesh density used while performing the analysis. It is hence imperative that we check the results obtained form numerical analysis using

experiments. This serves to validate the modeling approach that has been used. Two different techniques that are presently used in the research and industrial community to validate the modeling approach for electronic packages will be discussed in the subsequent sections.

2.8.1 Solder Ball Resistance Change Correlation

Qualification of electronic packages involves thermal cycling them in a thermal chamber and monitoring the resistance of a solder ball (or groups of solder balls called daisy chain) during thermal cycling. Failure is said to occur when the resistance of the solder ball increases from its initial value by a specific amount which is typically equal to 10% or 100%. Predictive models like Darveaux's however, give the correlation for the crack growth during thermal cycling. Crack growth in a solder ball cannot be measured directly during thermal cycling. Only the resistance change can be measured directly. It hence becomes necessary to relate the crack growth in a solder ball to its resistance change to be able to validate the results of numerical analysis with experimental ATC data.

Cracks in the solder ball typically originate from the fillet region as shown by the arrows in Figure 2.5.

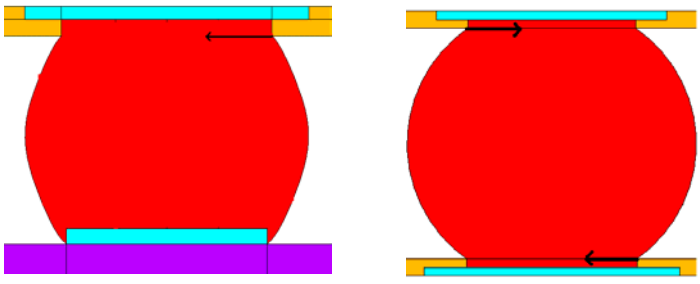


Figure 2.5 Crack growth direction in a solder ball for Solder Mask Defined (SMD) and Non-Solder Mask Defined (NSMD) pads

As shown in Figure 2.4, cracks might grow either on the package side or on the board side depending on whether the copper pad is solder mask defined or non-solder mask defined. Moreover, the solder ball being circular in cross-section, the relationship between crack growth and resistance of the solder ball during thermal cycling will not be linear. Numerical electrostatic analysis can be performed through FEA to determine the change in resistance of the solder ball as a function of crack growth. Similarly, numerical thermo-mechanical analysis in conjunction with Darveaux's model can be used to determine the crack growth in the solder ball as a function of number of cycles. The results from both the analysis can be combined to obtain the resistance change of the solder ball as a function of number of cycles. With the result obtained, validating the experimental results will be straightforward. Figure 2.6 illustrates this method through a flowchart.

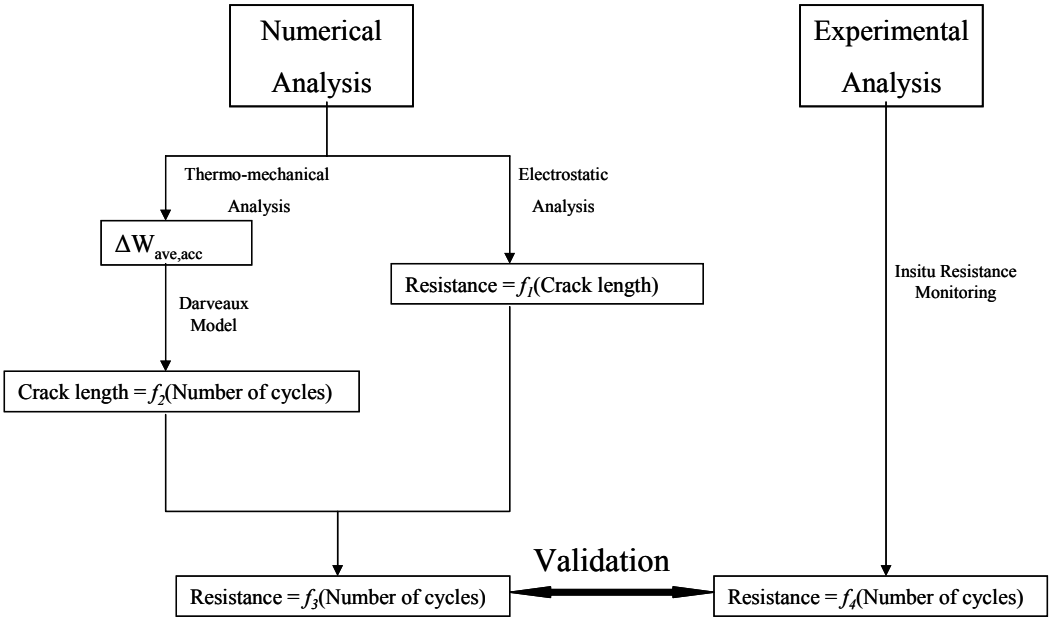


Figure 2.6 Model validation using resistance change correlation

It is a common practice that if the number of solder balls in a package is very large, the solder balls are connected in series with each other to form a daisy chain structure. In such a case, the resistance of the solder ball corresponding to the ones in the daisy chain should be found out from numerical analysis and should be added to each other before comparing with the resistance obtained from numerical analysis.

2.8.2. Moire Interferometry

Thermal and mechanical strains are a major cause of failure in the solder joints of many electronic assemblies. As the size of these interconnections decrease, the strain gradient increases and it becomes increasingly difficult to measure the strain gradients with high accuracy at such places. Moire interferometry techniques are relatively new and they have been extensively used to measure the displacements, strain and strain gradient present in electronic packages.

Moire interferometry is an optical method which provides whole field contour maps of in-plane displacements with a sensitivity as low as 0.417μm. A schematic diagram of the setting used for moiré interferometry is shown in Figure 2.7 [Han and Guo, 1995].

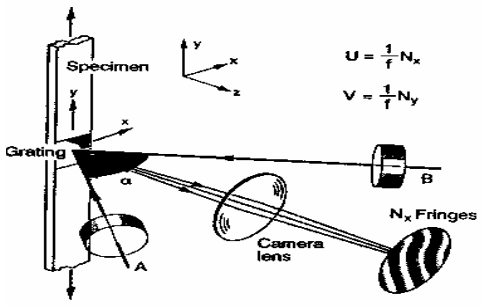


Figure 2.7 Schematic of moiré interferometry

The procedure involves replicating a high frequency crossed-line diffraction grating with ultra low CTE on the surface of the specimen so that it deforms together with the specimen when the specimen is subjected to either mechanical or thermal loads. An epoxy mold is used to transfer the grating onto the specimen as shown in Figure 2.8. The grating can be applied either inside an oven at elevated temperature or at room temperature. The detailed procedure for grating replication has been explained by Han (1994).

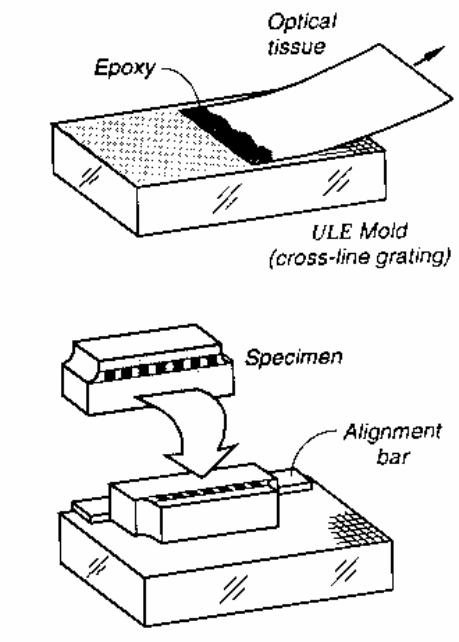


Figure 2.8 Sample preparation for moiré interferometry

Coherent beams *A* and *B* when incident on the grating as shown in Figure 2.7, create a virtual reference grating in their zone of intersection. When the specimen deforms, the grating also deforms with it. This deformed grating interacts with the virtual reference grating to produce the moiré interference pattern. Since the beams *A* and *B* are incident in the horizontal direction, vertical fringes are produced and these fringes are termed as U field fringes. Analogous

beams in the vertical plane would create another virtual reference grating which interacts with the second set of lines, perpendicular to the first one, to create the V field fringes. Figure 2.9 shows a sample of the U and V fields that are observed in a PBGA package when a thermal load of 60°C is applied to the package.

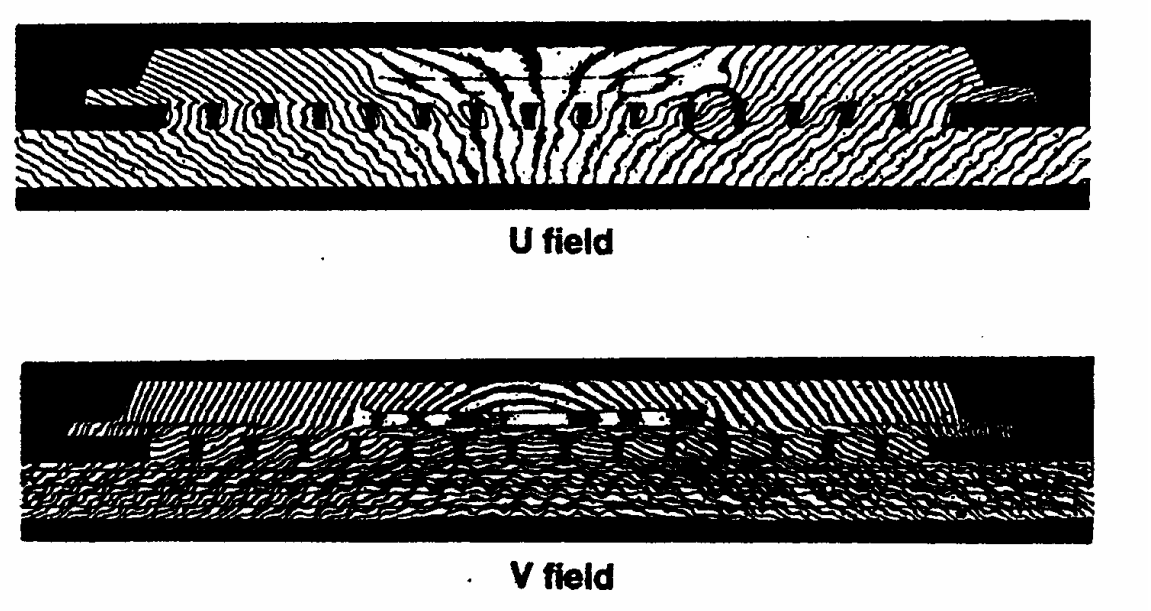


Figure 2.9 U and V fields in a PBGA package

The displacements can then be determined by the fringes by using the relations given in equation 2.20 [Dai et al, 1990].

$$U = \frac{N_x}{f}, \quad V = \frac{N_y}{f} \qquad \text{Eq (2.20)}$$

where, N_x and N_y are the fringe orders in the *U* and *V* field moiré patterns respectively. *f* is frequency of virtual reference grating and is given by equation 2.21.

$$f = \frac{2}{\lambda}\sin\alpha \qquad \text{Eq (2.21)}$$

where, λ is the wavelength of the light used for the coherent beam and a is the angle at which the coherent beam is incident. It should be noted that in moiré interferometry, the frequency of virtual grating is related to the cross-line grating frequency by the relation shown in equation 2.22.

$$f_s = \frac{f}{2} \qquad \text{Eq (2.22)}$$

where, f_s is the number of lines per millimeter length in the cross-line grating.

Once the grating has been applied, the *U* field fringes and *V* field fringes can be compared to the *U* and *V* displacements obtained from FEA at various temperatures. Moire interferometry can thus be implemented to validate the results obtained from Finite Element method.

2.9 Damage Metric Mapping

The temperature range, time of dwell, ramp rate and the number of cycles used for qualifying a microelectronic package should be based on the type of application the package is intended for. However, in the absence of specific guidelines, industrial practice is to subject the devices to legacy qualification cycles without ample consideration for the application of the product. If the qualification testing is excessive, then the packages may be over-designed and thus the design may be too costly and may sacrifice electrical and thermal performance for reliability.

To address the above mentioned problems, this paper follows a physics-based approach that maps the solder degradation or damage under field-use conditions with the solder degradation or damage under accelerated

thermal cycling (ATC) conditions. Two different mapping methodologies – linear and non-linear - will be dealt with to determine the number of ATC required for qualifying a package. Both strain-based and energy-based modeling approaches will be considered.

2.9.1 Linear Damage Mapping

Linear damage mapping is based on the assumption that the number of cycles to failure is inversely proportional to the inelastic strain energy density or to the inelastic strain accumulated in one thermal cycle. When summed over the number of cycles, these accumulated strain and accumulated energy density values are indicators of total amount of damage accumulated in the solder joint over an extended period of thermal loading. However, the accelerated values should not be taken as an indicator of the physical deformation of the solder joint. Linear mapping linearly sums the damage metric over the entire field-use. By dividing this summed damage metric by the damage metric in one ATC, the number of ATCs required to qualify a package is determined. Clearly, this approach of linear summation does not account for:

- Order in which the thermal loading is applied
- Change in material constitutive behavior

Although the order-sequence and the change in material constitutive behavior during field-use are critical to understand the evolution of solder damage, the linear summation approach provides an easy-to-use cumulative approach. Such an approach is useful especially when the loading conditions

are random or when a clear relationship between field-use conditions and damage is not well established.

The field-use conditions can often be broken down into similar operating conditions based on seasons, temperature range experienced etc. If p_i represents the number of cycles that the package experiences under each such operating conditions, then the number of cycles required to qualify a package by energy and strain based criterion is given by equations 2.23 and 2.24 respectively.

$$N_E{}^l = \frac{\sum_i p_i (\Delta W_{ave,acc})_i}{(\Delta W_{ave,acc})_{ATC}} \qquad \text{Eq (2.23)}$$

$$N_S{}^l = \frac{\sum_i p_i (\Delta \varepsilon^{in}{}_{ave,acc})_i}{(\Delta \varepsilon^{in}{}_{ave,acc})_{ATC}} \qquad \text{Eq (2.24)}$$

2.9.2 Non-Linear Damage Mapping

Non-linear damage mapping methodology is based on non-linear fatigue life and is implemented by using the relation existing between number of cycles to failure and the corresponding damage metrics. If N_f represents the failure life of a package then the damage occurring in the solder due to one cycle is defined by equation 2.25.

$$D = \frac{1}{N_f} \qquad \text{Eq (2.25)}$$

Here, N_f can take the form as given in equation 2.17, 2.18 or 2.19. The strain based and energy based non-liner mapping methodology will be discussed below.

Strain-Based Non-linear Mapping Methodology:

The strain-based non-linear mapping method that has been used separates the damage occurring in the solder to creep part and plastic part. The creep part of the damage is obtained by using equation 2.18 in equation 2.25. The damage due to creep is then given by equation 2.26.

$$D_c = \frac{\Delta\gamma_{cr}}{8.9} \qquad \text{Eq (2.26)}$$

The damage due to plasticity can be obtained by using equation 2.17 with equation 2.25. The expression is given in equation 2.27.

$$D_p = \frac{1}{C^{\frac{1}{m}}(\Delta\varepsilon)^{\frac{-1}{m}}} \qquad \text{Eq (2.27)}$$

The total damage that the solder experiences is the sum of creep and plastic damage and is given by equation 2.28.

$$D_t = D_c + D_p = \frac{\Delta\gamma_{cr}}{8.9} + \frac{1}{C^{\frac{1}{m}}(\Delta\varepsilon)^{\frac{-1}{m}}} \qquad \text{Eq (2.28)}$$

The field-use conditions can often be broken down into similar operating conditions based on seasons, temperature range experienced etc. If p_i represents the number of cycles that the package experiences under each such operating conditions, then the number of cycles required to qualify a package by strain based criterion can be obtained by summing over the damages

occurring under the field-use conditions and dividing this sum by the damage occurring under one ATC. This relation is given in equation 2.29.

$$N_S^{nl} = \frac{\sum_i p_i D_{t_i}}{D_{t_{ATC}}} \qquad \text{Eq (2.29)}$$

Energy-Based Non-linear Mapping Methodology:

Energy-Based mapping methodology uses equation 2.19 to obtain the damage occurring in the solder during one cycle. Equation 2.30 shows the expression for this damage.

$$D_t = \frac{(0.13\Delta W_{acc,creep} + \Delta W_{acc,plastic})}{C} \qquad \text{Eq (2.30)}$$

As was done for the strain-based mapping, the number of cycles required to qualify a package is given by equation 2.31.

$$N_E^{nl} = \frac{\sum_i p_i D_{t_i}}{D_{t_{ATC}}} \qquad \text{Eq (2.31)}$$

CHAPTER III

OBJECTIVES AND APPROACH

BGA packages are increasingly being used in microsystems applications due to several advantages it offers over the conventional CBGA packages: smaller footprint, faster signal transmission, testability, reworkability, etc. The use of plastic BGA packages in automotive and aerospace applications, where harsh thermal environment prevail, is relatively new. Hence, an experimental and theoretical modeling program was developed to study the solder joint reliability of two Plastic BGA packages.

The kinetics of damage accumulation in the solder joints used in electronic packages is influenced not just by the solder composition but also by all the other materials used in the package. The current industrial practice for qualifying a package involves building and assembling prototype packages and subjecting them to extensive qualification tests. Such a build-and-test approach is time consuming, expensive and does not provide additional insight into the actual location or mechanism of failures. In the absence of specific guidelines, industry practice is to subject the sample to harsh military-standard qualification tests without much consideration for the application of the product. These military standard tests are excessive for packages that are not used in harsh conditions. Moreover, when the packages are subjected to temperature regimes that they are not likely to experience in the field, the failure mechanism can be different than what is actually observed during field-use. Hence, the

number of accelerated thermal cycles, the temperature range and the time of dwell used for qualifying a microelectronic package should be based on the type of application the package in intended for. Therefore, for any accelerated test design, in addition to mapping the damage accumulation during field-use and thermal cycling, one should ensure that the associated failure mechanisms during the thermal cycling of the solder joints should be as close as possible to the field-use conditions.

The specific objectives of the present work include:

1. To study the solder joint reliability of SBGA and PBGA packages using numerical analysis and to validate the modeling methodology with in-house experimental data.
2. To develop a damage metric based mapping methodology to determine the number of accelerated thermal cycles required to qualify an SBGA package under automotive field-use conditions.
3. To develop an alternate accelerated thermal cycling regime that will mimic the solder joint behavior under field-use conditions

To achieve the above objectives, the following approach was pursued in this work:

1. Physics-based numerical models were developed that take into consideration the time- , temperature-, and direction-dependent material properties.

2. Determined the deformation fields in the PBGA packages under various temperature conditions using laser moiré interferometry and correlated the experimental data with numerical analysis to validate the modeling procedure.
3. Conducted air-to-air accelerated thermal cycling reliability tests with in-situ resistance measurement capabilities to determine the SBGA solder joint fatigue life and used the experimental data to validate the damage-metric based fatigue life
4. Using inelastic strain and strain energy density based damage metrics, performed linear and non-linear mapping between automotive field-use conditions and accelerated thermal cycling conditions to determine the number of cycles required to qualify the package.
5. Separating time-dependent and time-independent deformation behavior of the solder material, developed an alternate thermal cycling regime that represents the actual deformation mechanism occurring in the solder joint during its field-use.

CHAPTER IV

VIRTUAL RELIABILITY ASSESSMENT OF PBGA PACKAGES

The present chapter deals with the geometric modeling details for the PBGA package. It is generally not possible to model the entire electronic packages due to time and cost constraints. Hence, approximations were made to represent the actual geometry of package. The approximations involve either modeling the package in 2D instead of 3D or modeling only a part of the package instead of the whole. This chapter describes the geometric modeling details for PBGA package.

4.1 PBGA Package Board Construction

The PBGA packages were mounted on a five layer PCB. As schematic of the five layer PCB is shown in Figure 4.1.

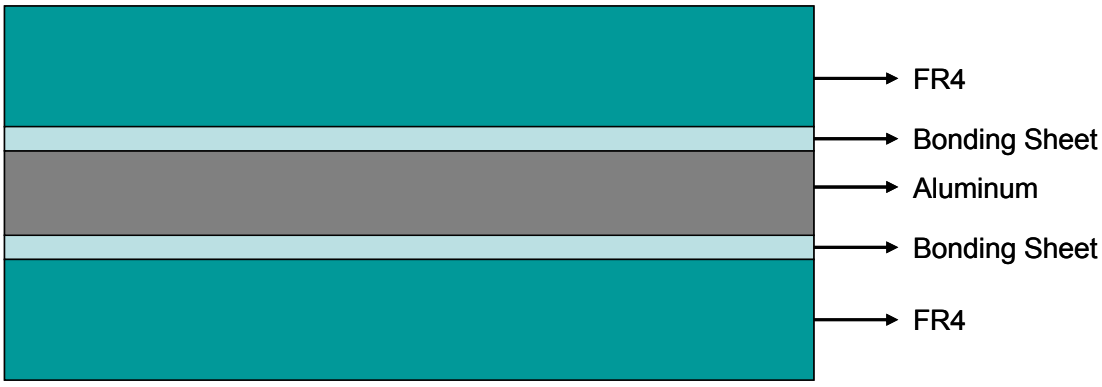


Figure 4.1 Schematic of the PWB used for PBGA package assembly

The five layers consist of two FR4 layers at top and bottom with a aluminum heat sink layer in the middle. Two rubber bonding sheets separate the

FR4 layers from the aluminum heat sink layer. The thicknesses of the five layers are given in Table 4.1. The five layers serve to provide a very high rigidity to the PCB.

Table 4.1 Thickness details of the PCB

Layer	Thickness (mm)
Bottom FR4	1.8796
Bottom bonding sheet	0.381
Aluminum heat sink	1.575
Top bonding sheet	0.381
Top FR4	1.8796

4.2 Geometric Details of PBGA Package

The Lattice™ PBGA 388 was used for the present work. A schematic of the PBGA package is shown in Figure 4.2. The package consists of a laminated substrate with layers of BT and copper. The IC faces upwards and the pads on the periphery of the IC are wire-bonded to the pads on the substrate. The IC and the wire-bonds are encapsulated with a mold compound. For the present work, the copper pads on the board side were non-solder mask defined and the copper pads on the package side were solder mask defined.

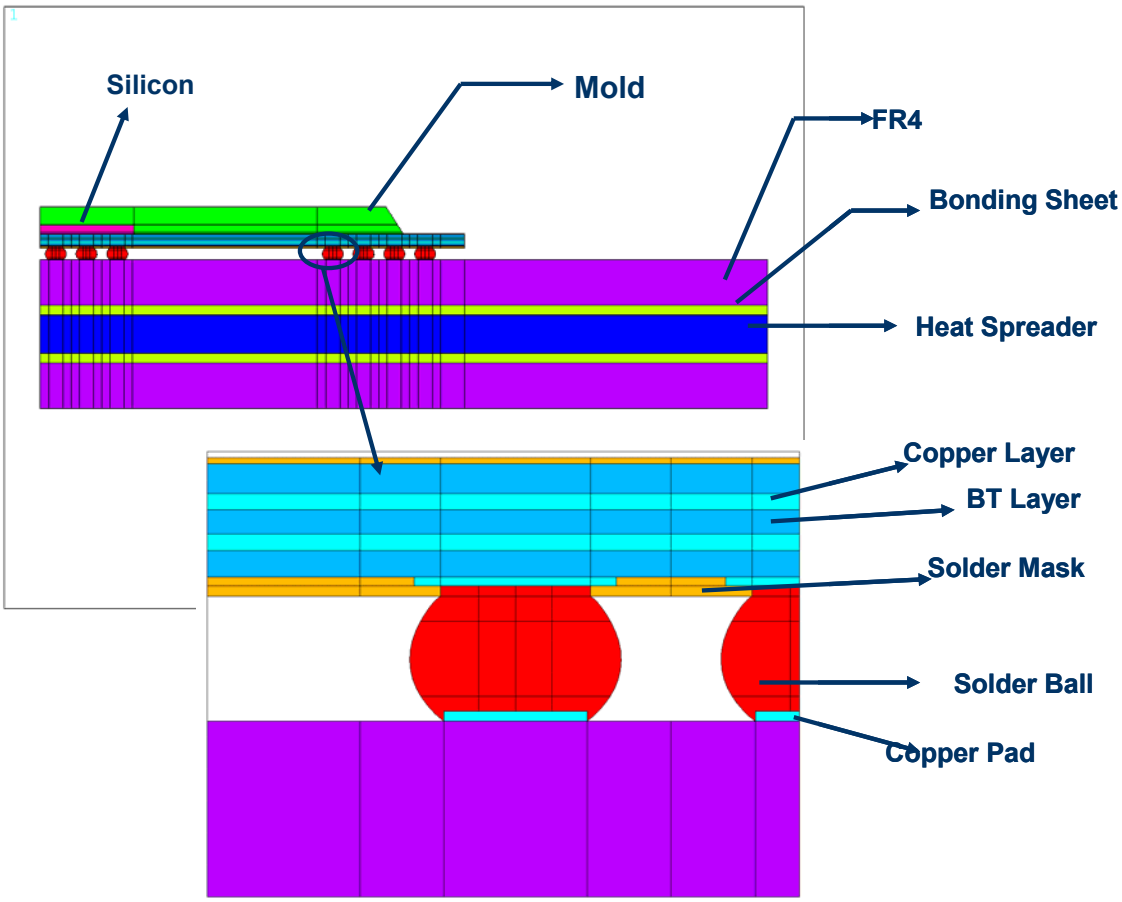


Figure 4.2 Schematic of Lattice 388 PBGA package

4.3 Geometric Models for the PBGA Package

4.3.1 2D Plane Strain Model

A plane strain model is the one in which the strains associated with the z-direction are zero. i.e,

$$\varepsilon_{zz} = \varepsilon_{xz} = \varepsilon_{yz} = 0 \qquad \text{Eq. (4.1)}$$

Plane strain conditions prevail when the dimension in the z-direction is infinite or significantly large compared to the x and y dimensions. When used to model an electronic package, a cross-section taken along the centerline of the

package is used for modeling purposes. 2D plane strain models reduce the computational time immensely compared to a 3D model. They can be used to quickly estimate the trend effects due to different underfills, solders, encapsulant, board thicknesses etc.

Firgure 4.3 shows the 2D Finite-Element meshed model of a PBGA package with the boundary conditions applied to it. The PBGA package is symmetric along the x-axis. Hence, only half the geometry is modeled. Symmetric boundary conditions exist at the left most edge. Therefore, all the nodes along this edge are constrained in the x-direction. The bottom left-corner node is constrained in all the directions to prevent rigid body motion.

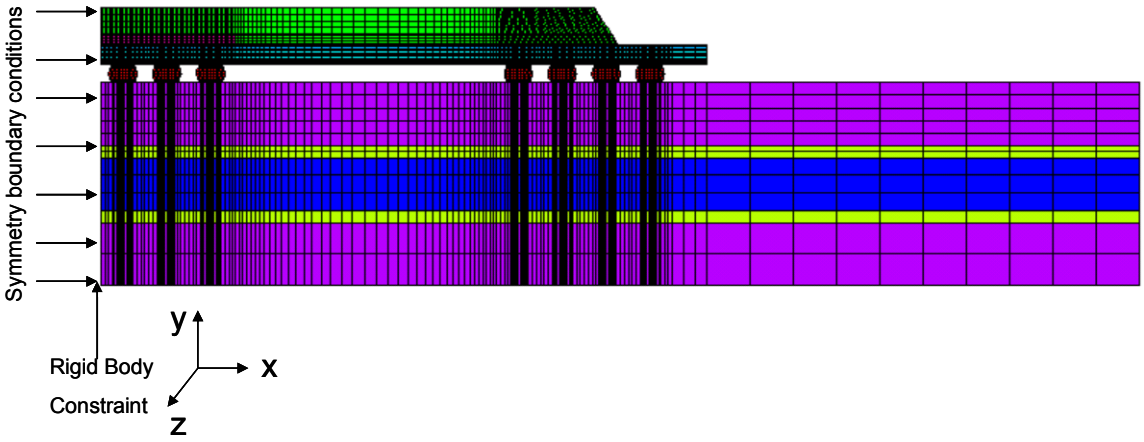


Figure 4.3 2D model of the Lattice 388 PBGA

4.3.2 3D Generalized Plane Deformation (GPD) Model

For thermo-mechanical analysis, the GPD model is a compromise between an accurate 3D model and computationally efficient 2D model. The geometry is represented by 3D elements which are used to represent only a part of the width of the whole package. For area array packages, the model width is equal to the pitch of the solder ball. This width would include only one solder ball

in the thickness direction as shown in Figure 4.4. The geometry of the solder ball was obtained using Surface Evolver. The Surface Evolver code that was implemented to obtain the geometry is given in Appendix A. Due to the symmetry of the package, only half of the package was modeled. Hence, all the nodes on the symmetry plane were constrained in the x-direction. A single node in the bottom left-corner was constrained in all three directions to prevent rigid body motion.

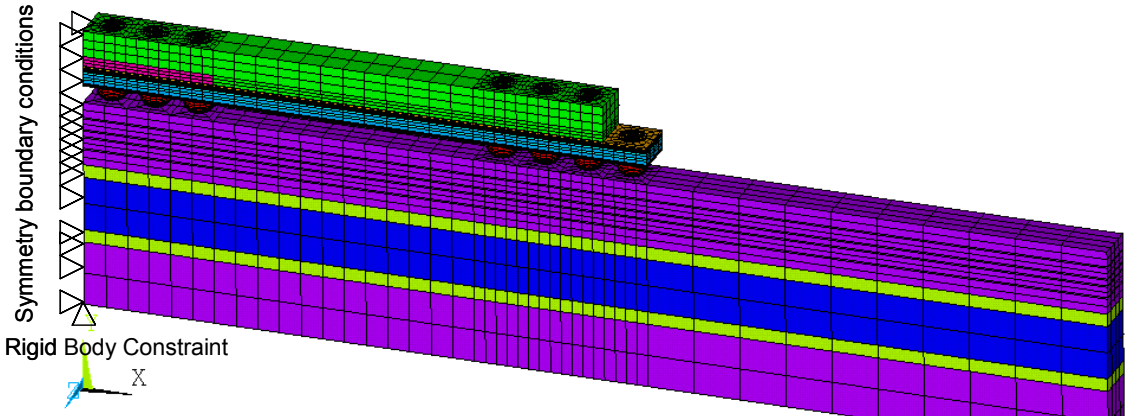


Figure 4.4 GPD model for Lattice 388 PBGA package

The two z-faces of the strip are coupled, as shown in Figure 4.5, so that all the nodes on these two faces move together in the same direction and by the same amount.

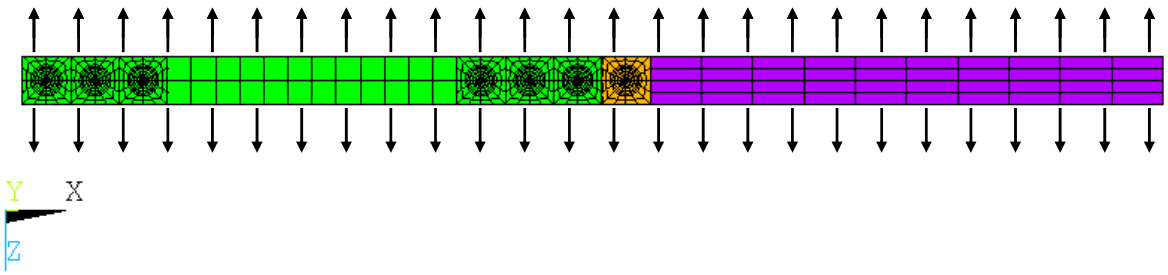


Figure 4.5 Coupled nodes in a GPD model

4.3.3 3D One Eighth Model

Full 3D model gives an accurate representation of the behavior of the package. But the computational time for running such a model is very high. However, if the 3D model possesses 1/8th symmetry, as shown in Figure 4.6, then the geometry size can be reduced by a factor of eight using the symmetry boundary conditions shown in the Figure.

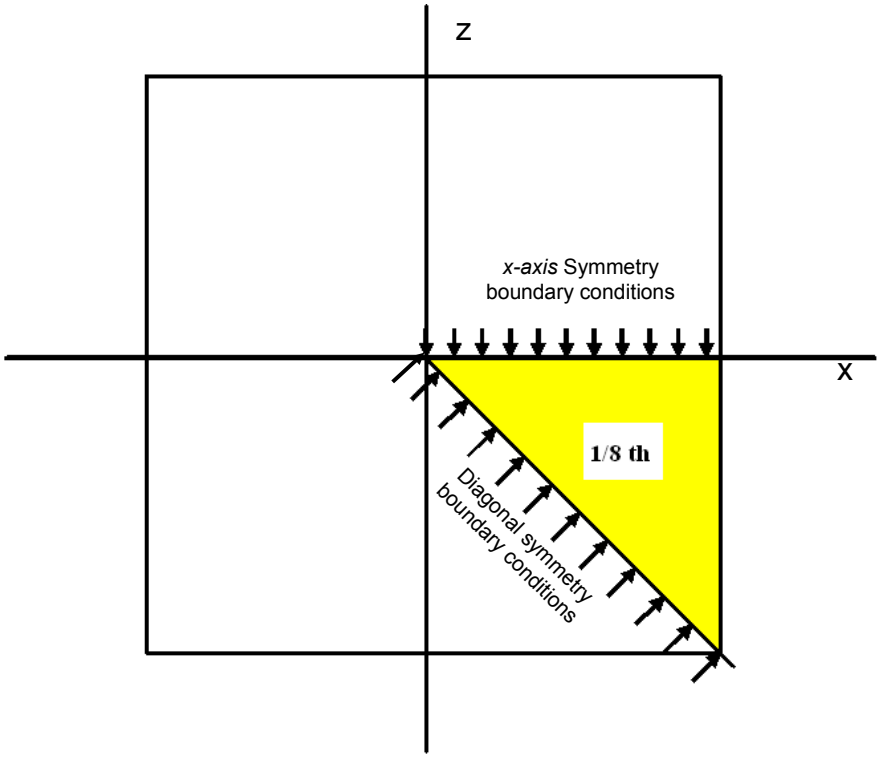


Figure 4.6 Slice of one eighth model

Figure 4.7 shows the one eighth model for the Lattice 388 PBGA. All the nodes at the left most edge are constrained with symmetry boundary condition. Finally, a single node at the bottom left-corner is constrained in all three directions to prevent rigid body motion.

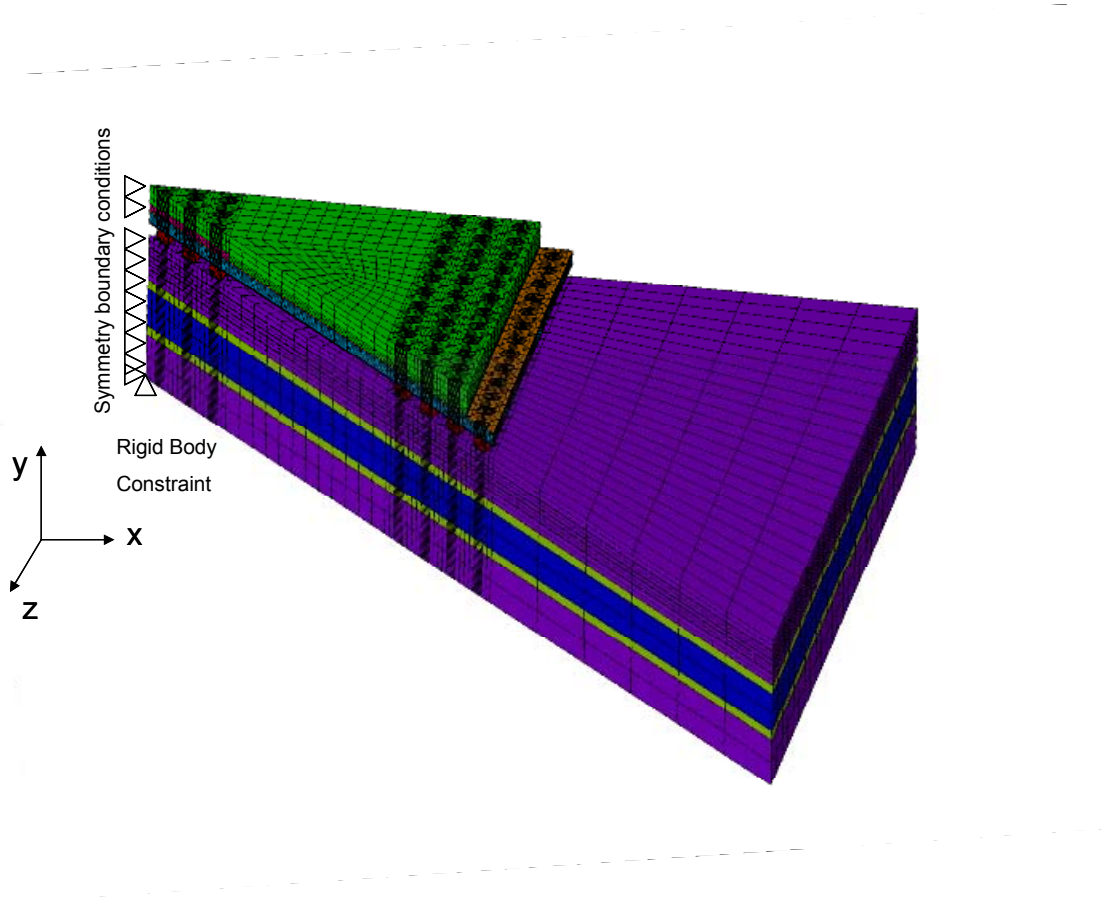


Figure 4.7 One eighth model

Surface Evolver software program was used to determine the shape of the solder ball for the 2D, GPD and 3D geometric models. The code that was implemented in Surface Evolver to obtain the solder geometry is given in Appendix A.

4.4 Material Models for the PBGA Package

PBGA packages use a combination of many different materials. The accuracy of the results from numerical analysis depends on the accuracy of the material models used. Since, solder joint fatigue is of primary interest in the present work, the solder material was modeled in detail using non-linear rate and temperature dependent material properties. All organic materials were modeled

using linear elastic material properties. Manufacturer supplied data was used wherever applicable. Table 4.2 lists the materials that were used to model the PBGA package.

Table 4.2 Materials used in the PBGA package

Part Name	Material
Package substrate	BT and Copper
Solder Mask	Epoxy
Solder Balls	62Sn/36Pb/2Ag solder
Mold	Epoxy
Die Attach Material	Silver Filled Epoxy
Die	Silicon
Board	FR4 with Rubber bonding sheets and Aluminum core

BT was modeled using isotropic linear elastic with orthotropic CTE. Table 4.3 shows the material property used for BT [BAE Systems, 2003].

Table 4.3 Material properties of BT

Material	BT
Property	Value
E, MPa	1.86×10^5
ν	0.36
G, MPa	6.84×10^4
α_x (10^{-6}/°C)	15
α_z (10^{-6}/°C)	15
α_y (10^{-6}/°C)	51

The FR4 used in the PCB was modeled as being temperature dependent orthotropic and linear elastic. Table 4.4 lists the material properties of FR4 that was used for modeling.

Table 4.4 Material properties of FR4 [Barker and Dasgupta, 1993, Michaelides, 1999]

T, °C	30	95	110	125	150	270
E_x (MPa)	22400	20680	19970	19300	17920	16000
E_z (MPa)	22400	20680	19970	19300	17920	16000
E_y (MPa)	1600	1200	1100	1000	600	450
ν_{xz}	0.136	0.136	0.136	0.136	0.136	0.136
ν_{xy}	0.1425	0.1425	0.1425	0.1425	0.1425	0.1425
ν_{yz}	0.1425	0.1425	0.1425	0.1425	0.1425	0.1425
G_{xz} (MPa)	630	600	550	500	450	441
G_{xy} (MPa)	199	189	173	157	142	139.3
G_{yz} (MPa)	199	189	173	157	142	139.3
α_x (10^{-6}/°C)	20	20	20	20	20	20
α_z (10^{-6}/°C)	20	20	20	20	20	20
α_y (10^{-6}/°C)	86.5	86.5	243	400	400	400

The solder mask was modeled as being temperature dependent isotropic with linear elastic properties [Schubert et al, 1997]. Table 4.5 lists the material properties of the solder mask that was used for modeling.

Table 4.5 Material properties for solder mask material [Cindas, 1995]

T, °C	-55	22	70	100	150
E, MPa	6000	4100	1420	330	100
ν	0.34	0.38	0.45	0.49	0.49
α_x (10^{-6}/°C)	36	36	36	36	36
α_z (10^{-6}/°C)	isotropic				
α_y (10^{-6}/°C)					

The material property for silicon was obtained from the data sheets provided by the manufacturer. Table 4.6 lists the material properties.

Table 4.6 Linear elastic material properties for silicon die

Material	Silicon
Property	Value
E, MPa	1.60×10^5
ν	0.23
α_x (10^{-6}/°C)	2.6
α_z (10^{-6}/°C)	isotropic
α_y (10^{-6}/°C)	

The rubber bonding sheet was modeled using temperature independent linear elastic isotropic properties. Table 4.7 lists the material property that was used for the rubber bonding pad [SRC/Cindas, 1999].

Table 4.7 Material property for rubber bonding pad

Material	Rubber bonding pad
Property	Value
E, MPa	2.068×10^3
ν	0.48
α_x (10^{-6}/°C)	220
α_z (10^{-6}/°C)	Isotropic
α_y (10^{-6}/°C)	

The aluminum core was modeled using isotropic temperature independent bilinear kinematic hardening [SRC/Cindas, 1999]. Table 4.8 shows the details of the material model for the aluminum. Figure 4.8 shows the stress-strain curve for aluminum material.

Table 4.8 Material property for aluminum core

Material	Aluminum core
Property	Value
E, MPa	67×10^3
Tangent modulus, MPa	667
ν	0.35
α_x (10^{-6}/°C)	24
α_z (10^{-6}/°C)	Isotropic
α_y (10^{-6}/°C)	

The copper material was modeled using temperature independent multilinear kinematic hardening model. The electroplated copper is known to exhibit kinematic hardening through Bauschinger effect [Lubliner, 1990]. Table 4.9 shows the elastic material properties of copper and Figure 4.8 shows the stress-strain curve for the copper material [Iannuzzelli, 1991].

Table 4.9 Elastic material property of copper

Material	Copper
Property	Value
E, MPa	$121x10^3$
ν	0.3
$\alpha_x = \alpha_y = \alpha_z$ (10^{-6}/°C)	17.3

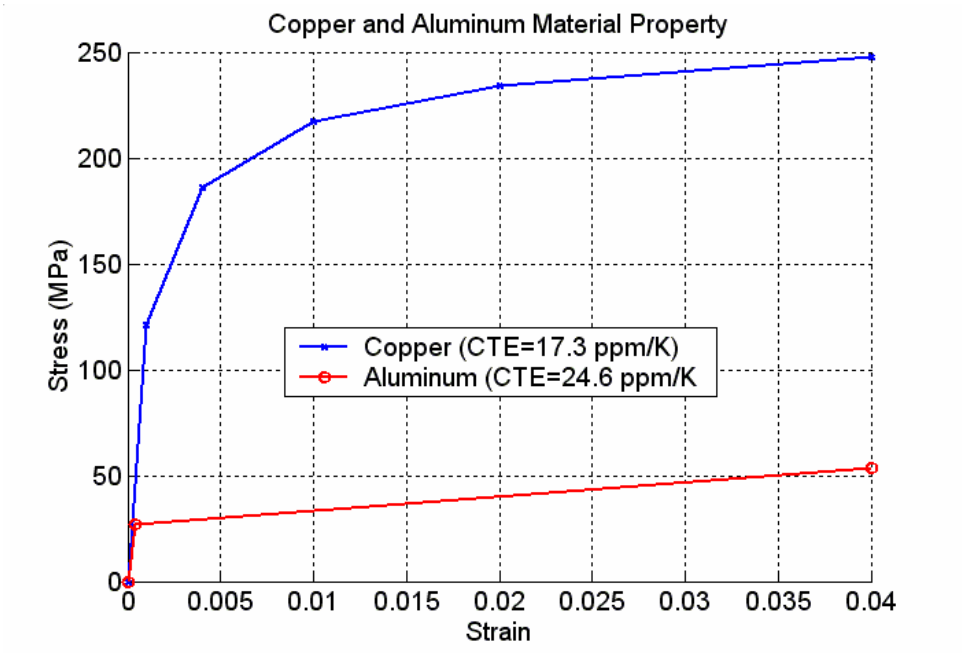


Figure 4.8 Stress-strain curve for copper and aluminum

Three different mold compounds were used for the PBGA packages. The names of the mold compounds are proprietary. The mold compounds are therefore called as MC 1, MC 2 and MC 3. The mold compounds were modeled as temperature dependent linear elastic isotropic material. Figure 4.9 and Figure 4.10 show the CTE and modulus information of the PBGA package. The poisson's ratio for all the mold materials were assumed to be 0.3.

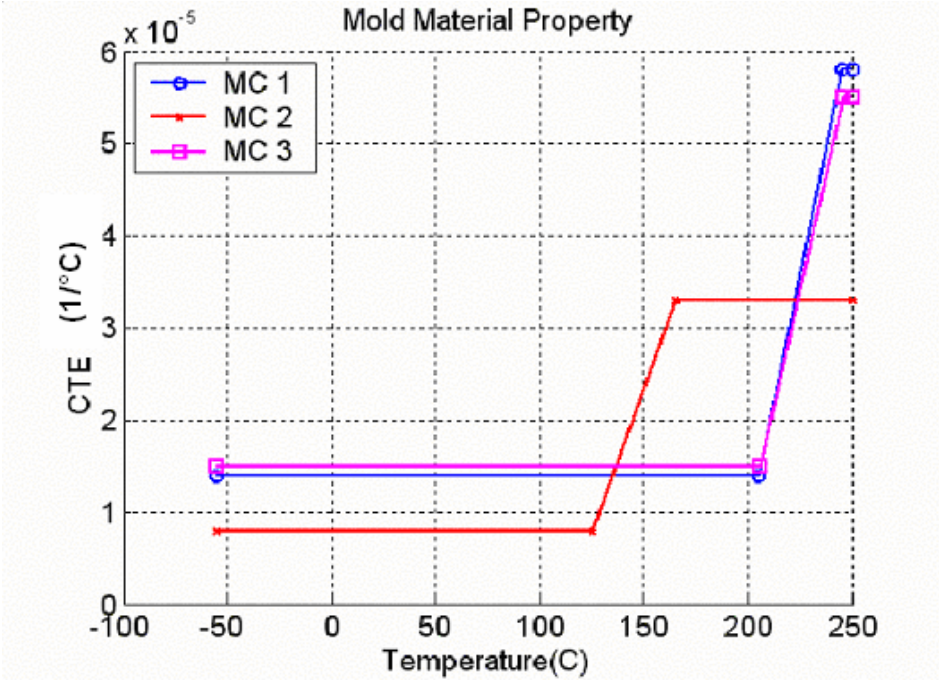


Figure 4.9 Variation of CTE for the mold compounds with temperature

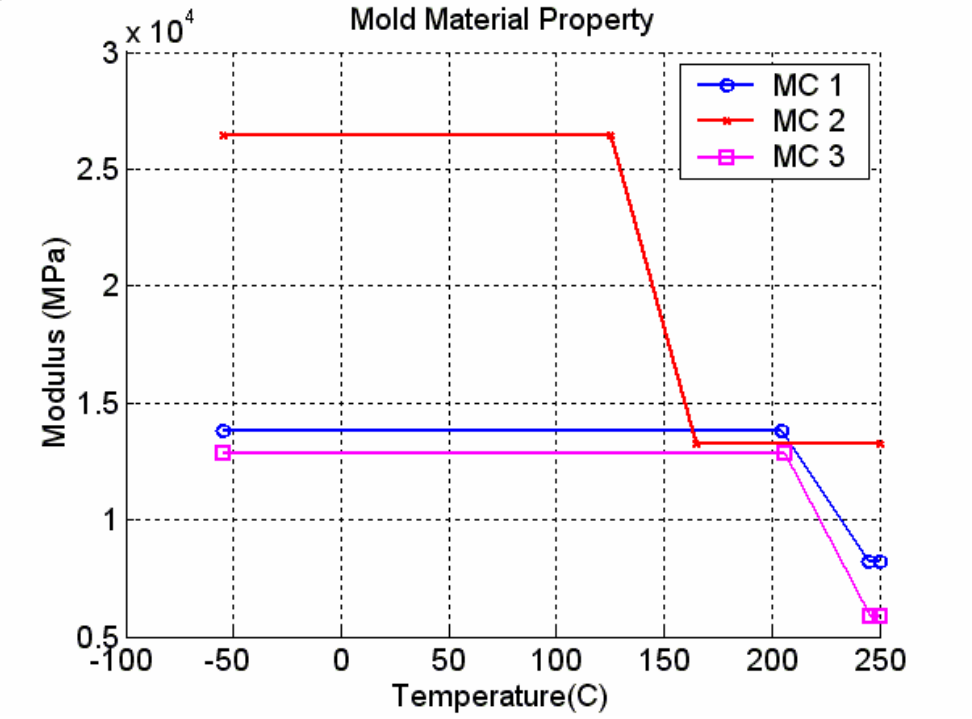


Figure 4.10 Variation of modulus for the mold compounds with temperature

Two different die attach materials were used for the modeling purposes. The material used for the die attach is a proprietary information. They are hence called as DA 1 and DA 2. These two die attach materials were modeled using temperature dependent linear elastic isotropic materials. Figure 4.11 and Figure 4.12 show the variation of the CTE and modulus with temperature for the die attach material.

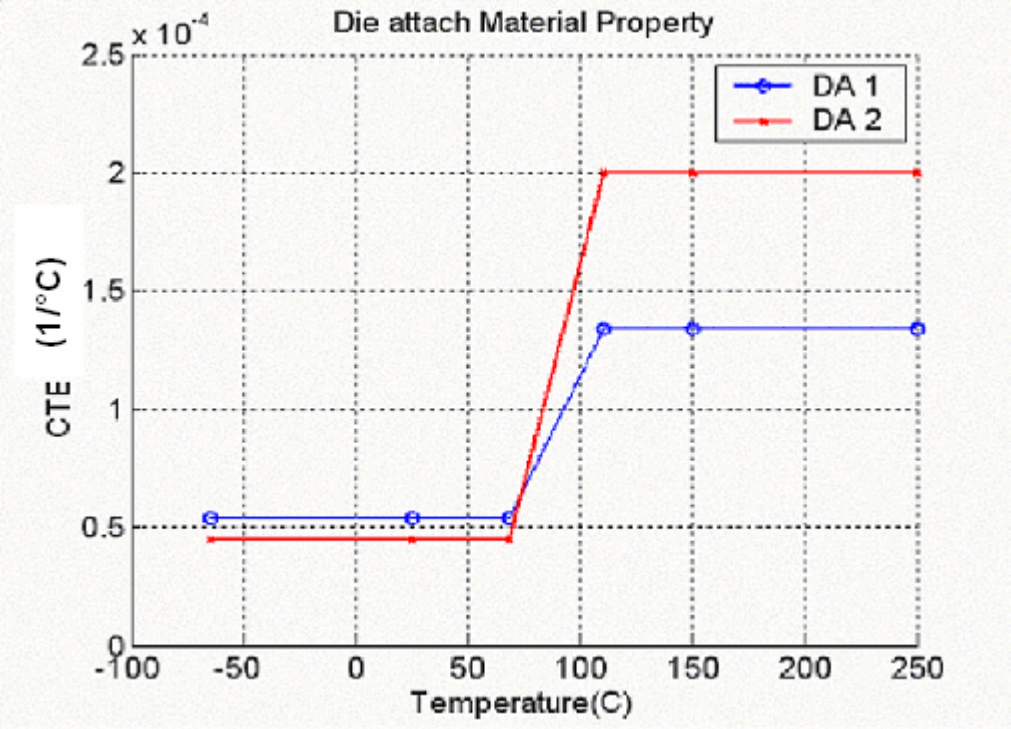


Figure 4.11 Variation of CTE for the die attach compounds with temperature

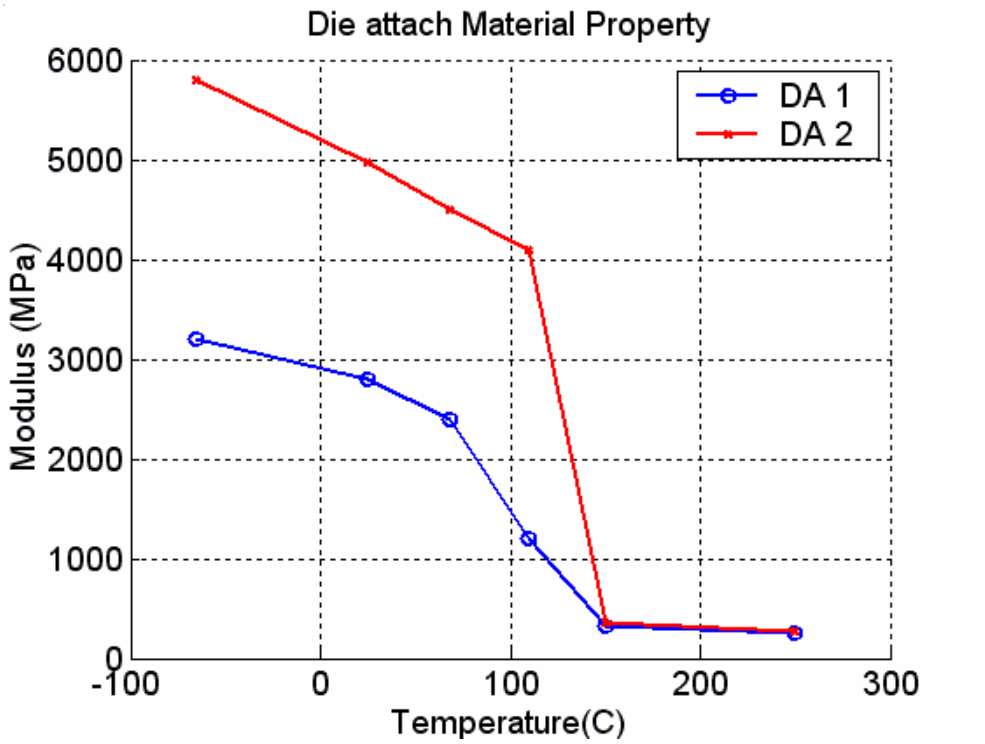


Figure 4.12 Variation of the modulus for the die attach compounds with temperature

4.5 Solder Material Models

Solder is a soft material and has a high homologous temperature even at room temperature. The deformation behavior of the solder material is hence highly rate dependent. The rate dependency is taken into account by modeling the solder material using unified viscoplastic model.

4.5.1 Viscoplastic Model for 62Sn/36Pb/2Ag Solder

Viscoplastic models do not separate the deformation mechanism into rate dependent and rate independent terms. The constants for the equation 2.7 to 2.9 are given in Table 4.10 [Darveaux, 1997]. Modeling viscoplasticity would also require elastic properties for the solder material.

Table 4.10 Constants for Anand's model for 62Sn/36Pb/2Ag solder

Meaning	Darveaux's Constants for Anand's Model
s_o, MPa	12.41 MPa
$Q/R, K$	9400 K
$A, \sec^{-1}$	$4.000\times10^{6}\cdot\sec^{-1}$
ξ	1.5
m	0.303
h_o, MPa	1379 MPa
$\hat{s}, MPa$	13.79 MPa
n	0.07
a	1.3

The shear modulus of the solder material was found according to the equation 4.1.

$$G(T) = G_o - G_1 T \qquad \text{Eq(4.1)}$$

Where *G* is the shear modulus of the solder material, *T* is the temperature in °C, G_o and G_1 are material constants. The constants for G_o and G_1 are shown in Table 4.11 [Darveaux and Banerji, 1992]. The CTE and poisson's ratio of the material was assumed to be $24.5\text{x}10^{-6}$/K and 0.35 respectively.

Table 4.11 Constants for the elasto model

G_o, 10^6 psi	G_1,10^3 psi
1.9	8.1
G_o, MPa	G_1, MPa
1.3×10^{4}	56

4.6 Thermo-mechanical Analysis of the PBGA Package

Numerical models in conjunction with life-prediction models can be used to determine the number of cycles to solder joint fatigue failure under thermal cycling. This section summarizes the results from the 2D, 3D and GPD models that were created for a PBGA 388 package.

As was outlined in section 4.4, the PBGA package used one of the three mold compounds and one of the two die-attach compounds. Hence, a preliminary 2D plane strain analysis was performed using the six possible combinations of die-attach and mold compounds to assess the worst-case combination.

The solder melting temperature of 183°C was assumed as the stress free temperature for the model. The package was first subjected to a load step from 183°C to room temperature and then allowed to dwell for about an hour at room temperature. Subsequently, the package was subjected to accelerated thermal cycling conditions in a thermal chamber from -55°C to 95°C with half hour dwell at each temperature extremes and half hour ramp between these two temperature extremes. Figure 4.13 shows the thermal profile used for simulating the thermal cycling conditions.

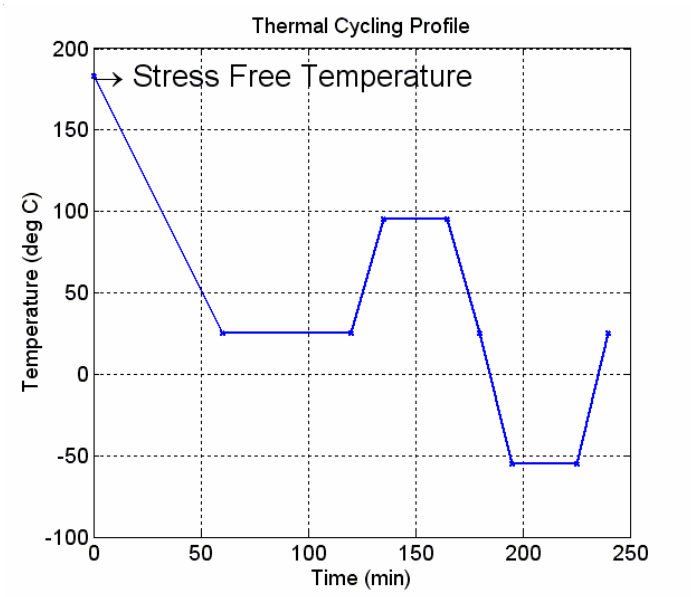


Figure 4.13 Thermal profile for a PBGA assembly

The accumulated plastic strain and plastic strain energy density were found to be higher at the package side of the solder ball than the board side of

the solder ball. Hence, the averaging for these strains and energy densities were done only at the package side of the solder. Figure 4.14 shows the convention used for averaging.

Figure 4.14 Averaging convention used for PBGA package

Figure 4.15 shows a plot of von Mises stress versus accumulated plastic strain for a typical element in the solder during thermal cycling. The package was subjected to several thermal cycles to ensure that stabilized results were obtained from each thermal cycle. The shaded area is the accumulated plastic strain energy density in one thermal cycle.

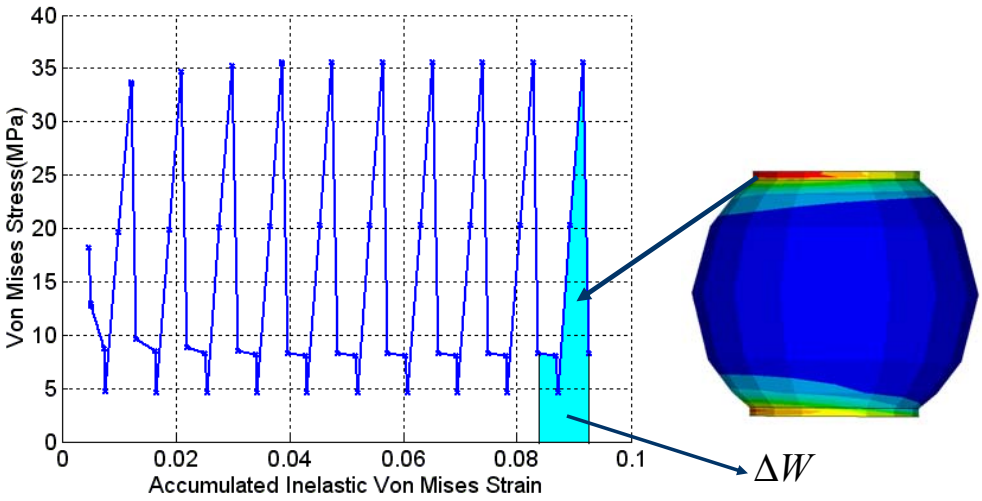


Figure 4.15 von Mises stress vs. accumulated inelastic von Mises strain for a typical element

Table 4.12 shows the area averaged plastic energy density accumulated in the worst-case solder ball in each of these six combinations. The area averaging was performed according to equation 2.11.

Table 4.12 Summary of 2D simulations for PBGA 388 package

Combination (Mold + Die-Attach)	Worst-case solder ball (Strip number)	Accumulated plastic energy density per cycle (N/mm^2)
MC 1 + DA 1	1	0.13968
MC 1 + DA 2	1	0.13927
MC 3 + DA 1	1	0.13865
MC 3 + DA 2	1	0.13826
MC 2+ DA 1	6	0.16650
MC 2 + DA 2	6	0.16654

It can be seen from Table 4.12 that the MC 2 in combination with the DA 2 adhesive was the worst among all the combinations. It can also be noticed that using MC 2 would cause the solder ball next to the outermost edge to fail whereas using the other two mold compounds would cause the solder ball in the inner most row, just under the die, to fail. 3D and GPD models were created based on the worst case combination which used the MC 2 compound with DA 2 die-attach material. Figure 4.16 shows the plot of accumulated inelastic work in one thermal cycle for the GPD model.

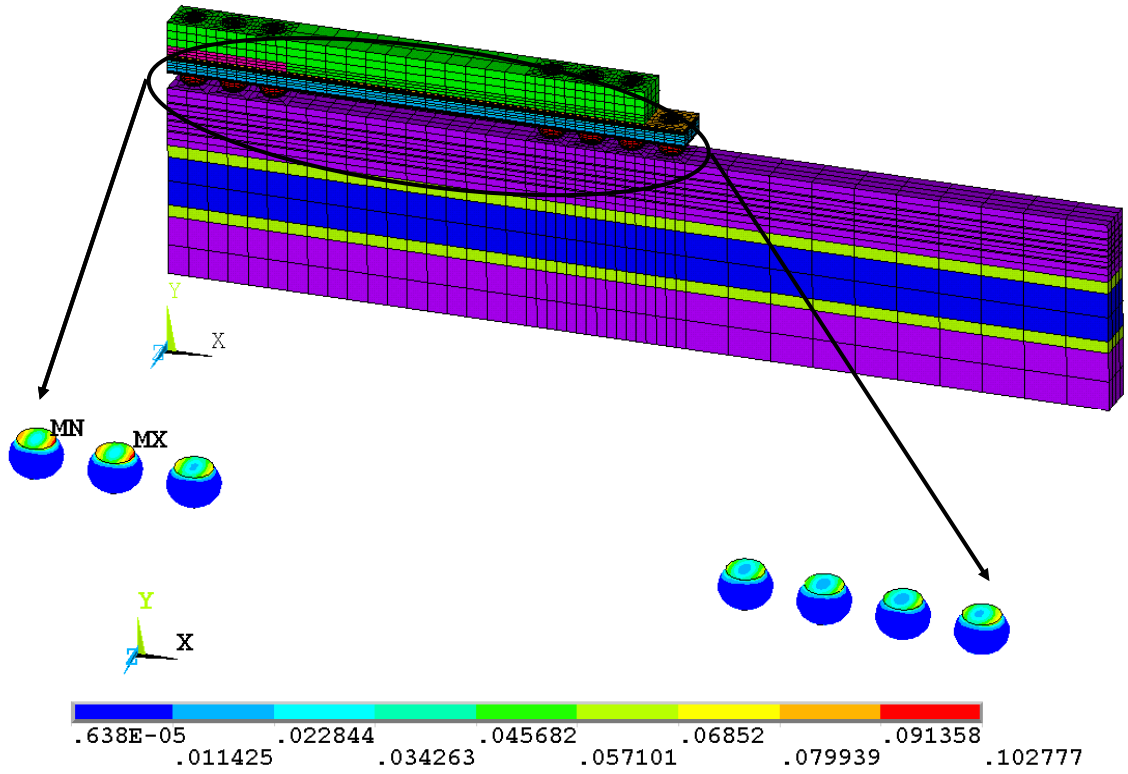


Figure 4.16 Accumulated inelastic work contours from the GPD model in N/mm^2

As can be seen from Figure 4.16, the maximum accumulated inelastic strain energy density was observed in the solder ball next under the die. Figure 4.17 shows the accumulated inelastic strain energy density contours for the 3D model. The maximum inelastic strain energy density was found to accumulate in the solder farthest from the neutral point along the diagonal line.

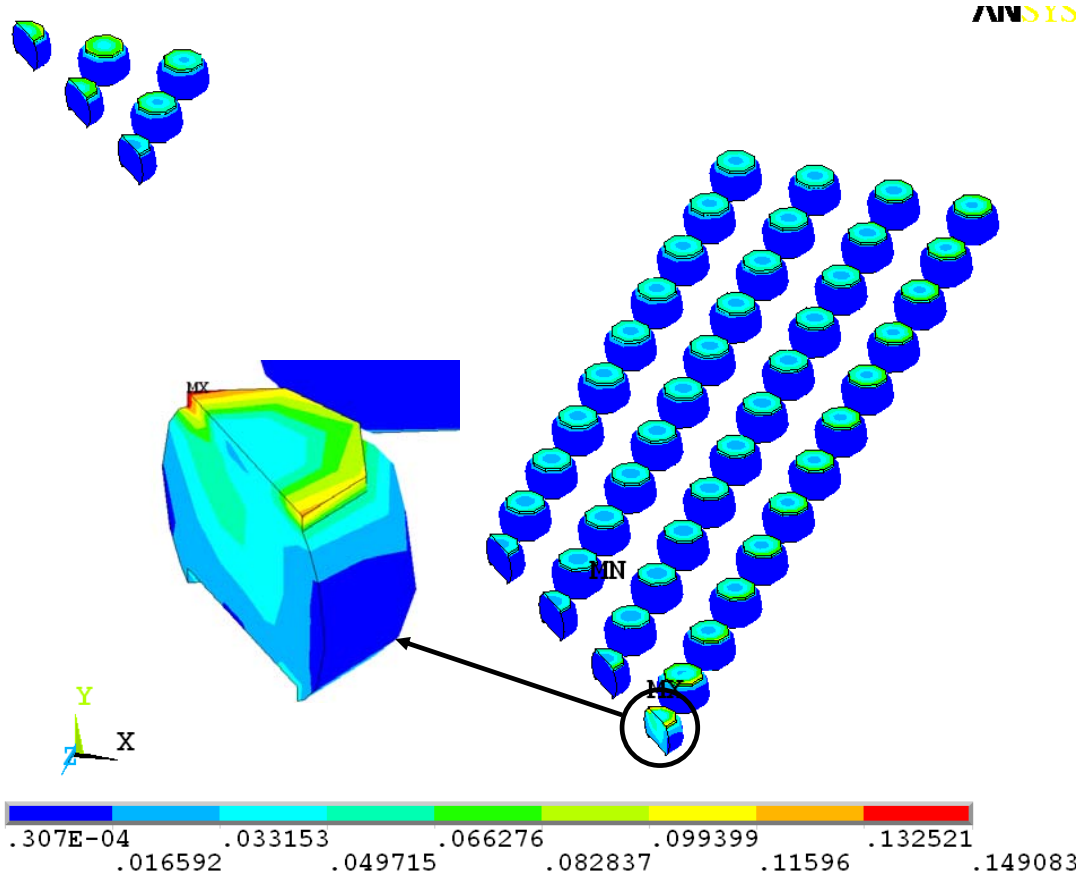


Figure 4.17 Accumulated inelastic work density contours for the 3D model in N/mm^2

The volume averaged accumulated inelastic strain energy density as determined by 2D, 3D and GPD model is given in Table 4.13.

Table 4.13 Accumulated inelastic work for various models

Geometry Model	Accumulated inelastic work density (N/mm^2)
2D plane strain	0.16654
GPD	0.04527
3D	0.06978

The 2D plane strain model is stiffer compared to GPD and the 3D model. Hence, the stresses in the 2D model is very high. These high stresses give rise to higher accumulation of plastic work. The GPD model however, is relatively fliexible compared to the 3D model. Hence, the stresses in the GPD model is not

as high as that of 3D model. Consequently, the plastic work accumulated is less than in the 3D model.

Using the results of the GPD model and 3D model from Table 4.13 with Darveaux's fatigue equations given by 2.12 and 2.16, the mean number of cycles to failure can be obtained. Since, the Darveaux equation was originally developed for 3D and GPD models and not for 2D models, the inelastic strain energy density determined by 2D model cannot be used for fatigue life estimation. The constants used for the Darveaux equations 2.12 and 2.13 are given in Table 4.15 [Darveaux, 2000]. It should be noted that the constants are different for the GPD model and for the 3D model. For the 3D model, the value of the constants, as reported by Darveaux (2000), depends on the thickness of the element layers at the interface between the solder and the copper pad. The 3D model that was created had the element thickness value at the interface as 0.855×10^{-3} inch. The constants were obtained by interpolating the constants provided by Darveaux (2000) for various element thicknesses.

Table 4.14 Constants used for the Darveaux model to determine fatigue life

Model	K1 (Cycles/MPa^{K2})	K2	K3 (mm/(cycles x MPa^{K4}))	K4
GPD	10.521	-1.52	0.00211356	0.990
3D	19.082	-1.62	0.00144419	1.043

Once the mean number of cycles to failure is obtained, the number of cycles for 1% failure can be estimated by using equation 2.16. Table 4.15 summarizes the mean and fatigue life estimates for the PBGA package as determined by the 3D and GPD model. The shape factor for the failure was assumed to be 5 based on commonly observed shape factors for PBGA packages [Lau and Pao, 1997].

Table 4.15 Fatigue life estimates for the PBGA package

Geometry Model	Mean number of cycles to failure	Number of cycles for 1% failure
GPD	7358	5145
3D	8226	5752

The fatigue life predicted by the GPD model matches closely with the fatigue life predicted by the 3D model. However, as was seen from Figures 4.16 and 4.17, the failure location predicted by the GPD model differs from the failure location predicted by the 3D model. We can therefore conclude that, to estimate the fatigue life, one can use either GPD model or 3D model. However, to determine the exact location where failure is going to occur, it is necessary to create a whole 3D model.

CHAPTER V

EXPERIMENTAL VALIDATION OF VIRTUAL RELIABILITY ASSESSMENT MODELS OF PBGA PACKAGES

Chapter IV provided details on the numerical modeling of PBGA packages. The results obtained from the analysis were also provided. This chapter provides a comparison between the deformation behavior of the solder joints as determined by numerical analysis and by moiré interferometry. This would serve to validate the model against experimental data.

5.1 PBGA Model Validation Using Moiré Interferometry

Validation of the results from FEA analysis is commonly done through accelerated thermal cycling. Thermal cycling does not provide details about the displacements and strains occurring in the solder joints. Moire interferometry on the other hand gives detailed information about the deformation occurring at the microscopic level in the solder joint as well as in other materials used in the package. Moire is thus a direct way of validating deformations and strains occurring in the package. The theory behind the working of moiré interferometry has been explained in section 2.8.2.

5.1.1 Geometric Model for Validation Study

Moire interferometry is an experimental technique used to verify the validity of the numerical analysis. The procedure involves cutting the package along the centerline so that it includes 2-3 rows of solder balls. The cut sample is

then polished through the rows of solder balls so that its cross-section is exposed. A grating is then applied on the polished surface and the sample is then subjected to thermal loading to monitor the strains and displacements that the solder balls experiences. To be able to validate the strains and displacements, numerical analysis should be performed on the geometry that matches with the geometry of the cut sample. Figure 5.1 shows the geometry of the sample that was used for moiré interferometry studies.

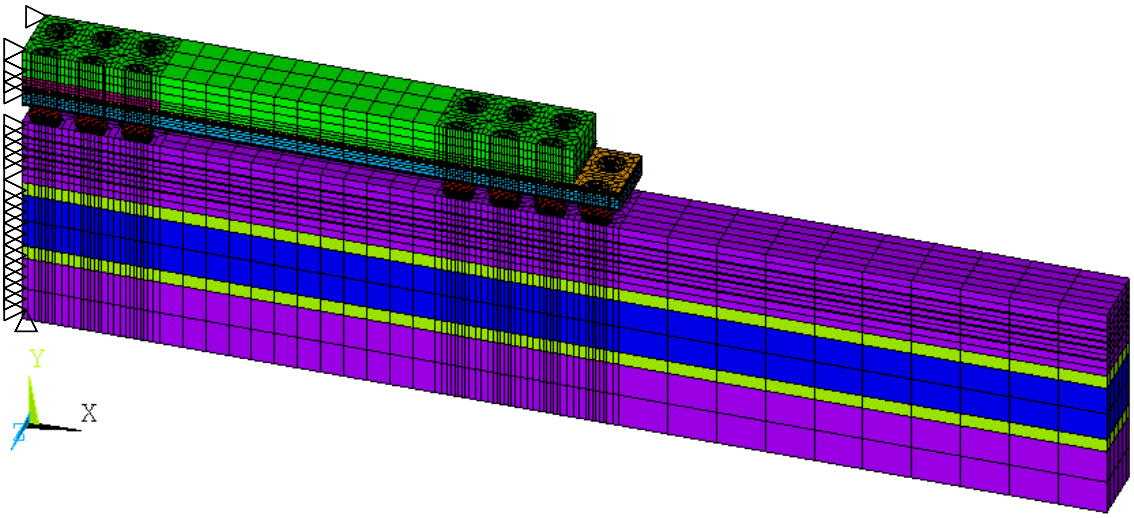


Figure 5.1 Sample used for moiré interferometry

The boundary conditions includes the symmetry boundary condition of constraining all the nodes on the left-most surface in the x-direction and constraining one node at the bottom left-most corner in all three directions to prevent rigid body motion.

5.1.2 Experimental Details for Moire Interferometry

The PBGA package was cut in the form of a thin strip with the thickness being equal to one and a half times the pitch. The grating that was used had a frequency of 1200 lines/mm which would give a resolution of 417 nm per fringe.

The grating was applied to the sample at room temperature, using an epoxy mold, as shown in Figure 2.8. The mold was allowed to cure at room temperature for three days and then the sample was pried off. The pried off sample now had a thin layer of grating coated onto it. The sample was then placed in a thermal chamber and a reference virtual grating was obtained at room temperature. Figure 5.2 and 5.3 show the *U* and *V* virtual reference grating that was obtained at a room temperature of 20°C. Ideally the U and V field virtual reference grating should have zero fringes. But the prying off process invariably induces some amount of residual strain in the package due to which few fringes are still present. It is difficult to get rid of these fringes.

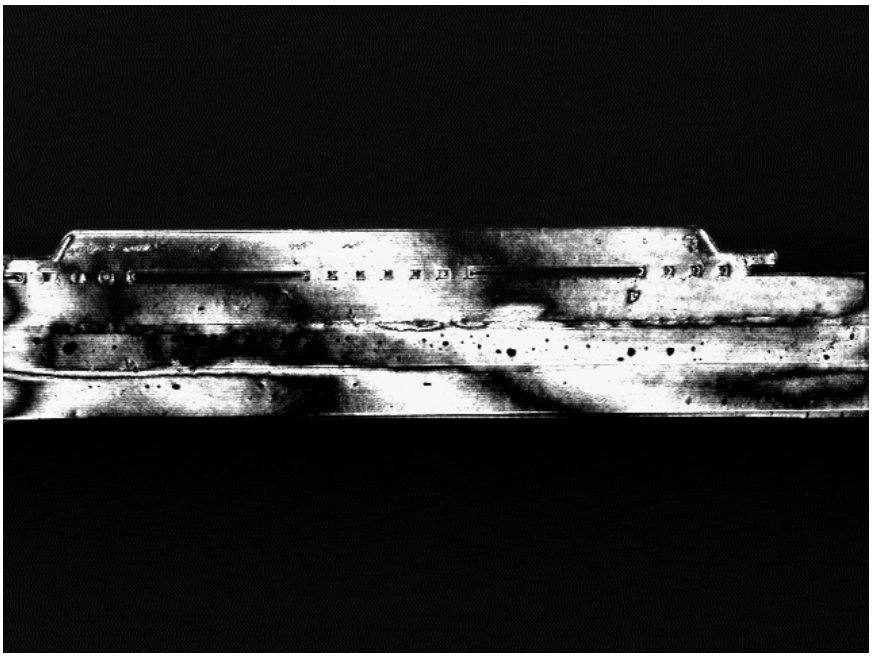


Figure 5.2 *U* field virtual reference grating

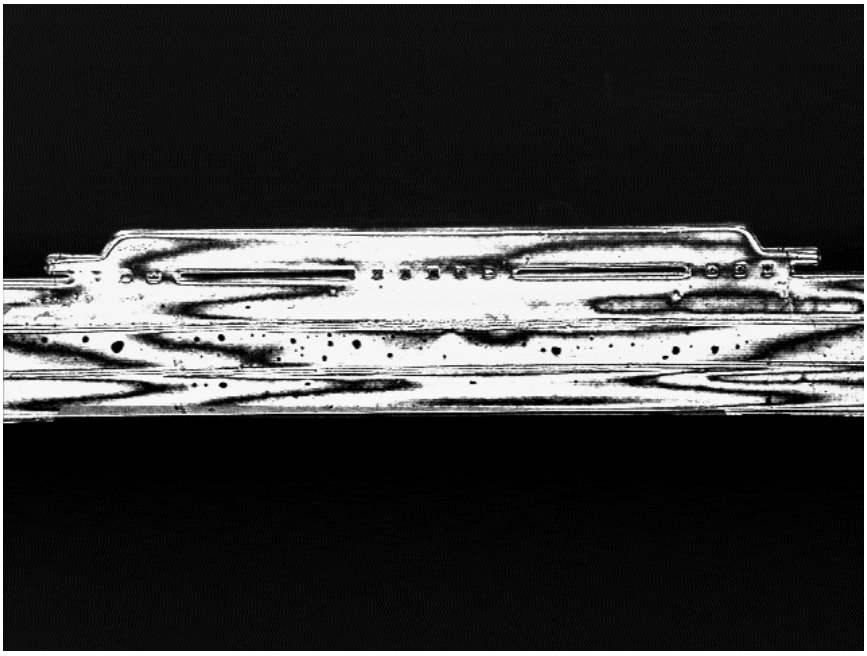


Figure 5.3 *V* field virtual reference grating

The thermal chamber was then cooled to -25°C at a rate of 5°C per minute and then heated to 100°C at about the same rate. The fringe pattern was recorded at -25°C, -10°C, 0°C and 100°C. At each designated temperature, the thermal chamber was allowed to dwell for about 10 minutes to make sure that the sample would reach the thermal chamber temperature. Finite element simulations were performed in parallel using the moiré geometry model.

5.1.3 Comparison of Results from Moire Interferometry and Geometric Modeling

The stress-free temperature was assumed to be 20°C, which was the temperature at which the grating was applied. Figures 5.4 through 5.5 show the fringe pattern in the *U* and *V* direction observed in moiré interferometry at each of these temperatures along with the contour plot of the displacement fringes obtained by FEA analysis.

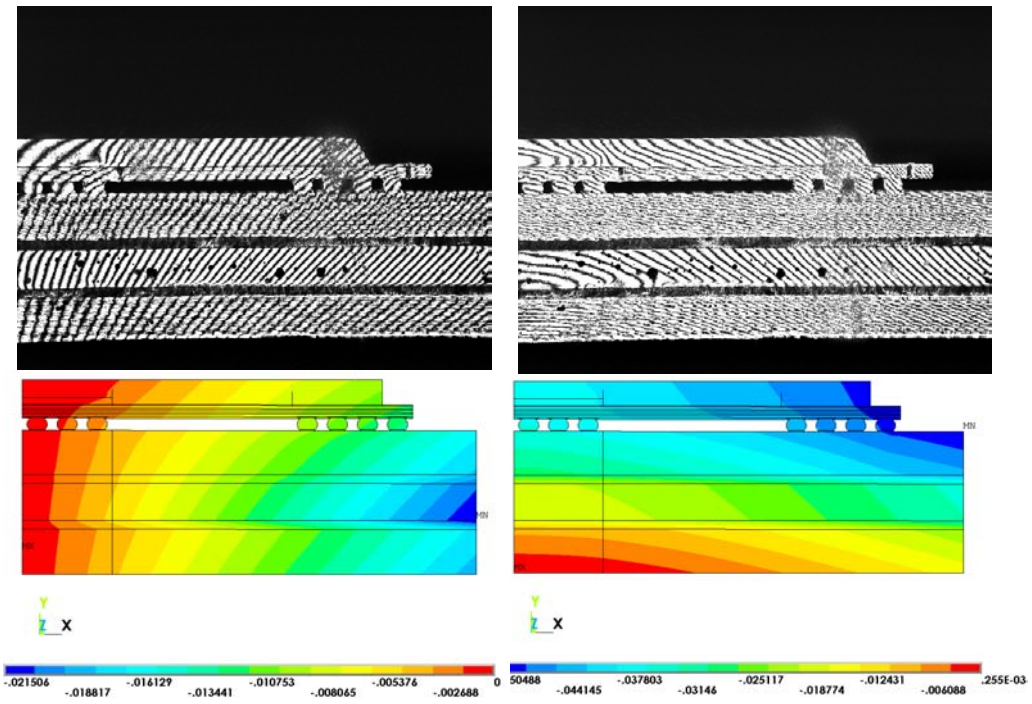


Figure 5.4 *U* and *V* field fringes at -25°C

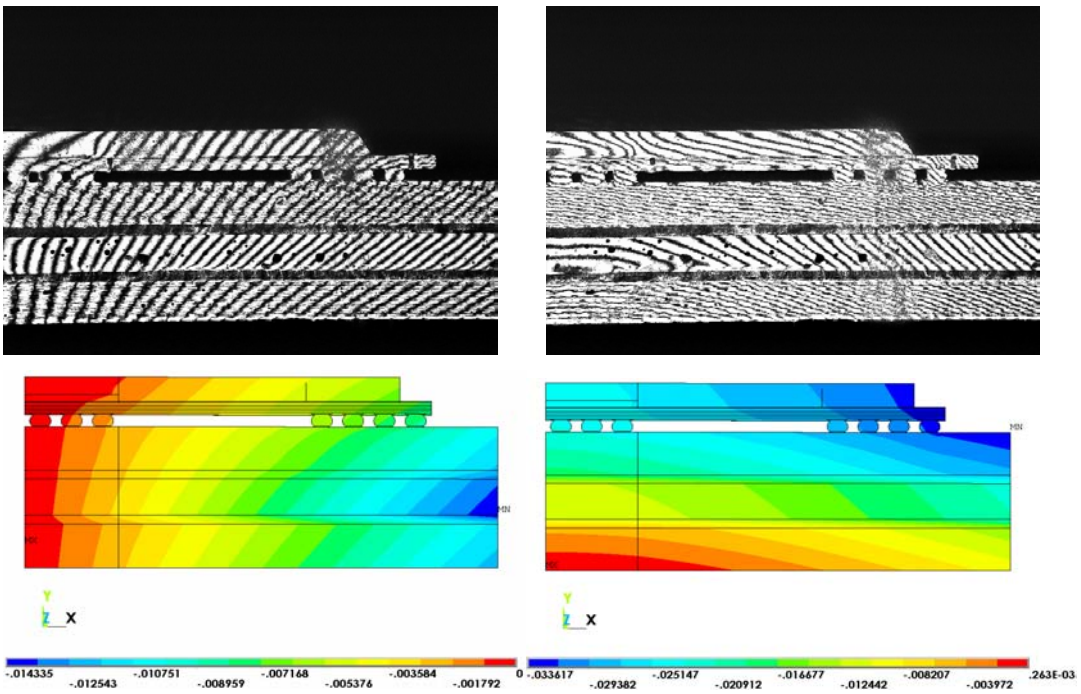
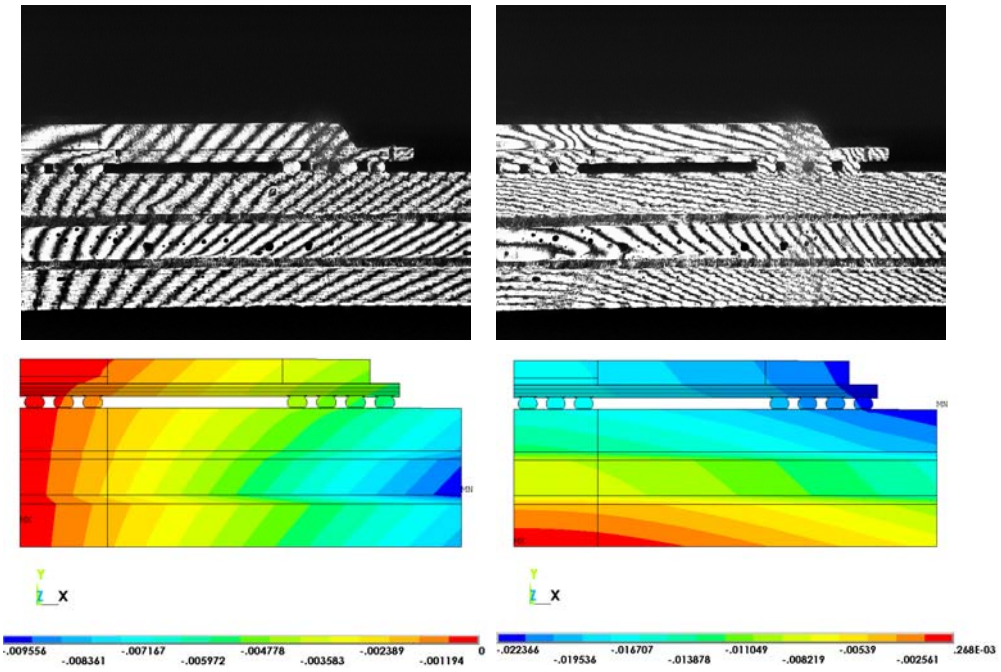
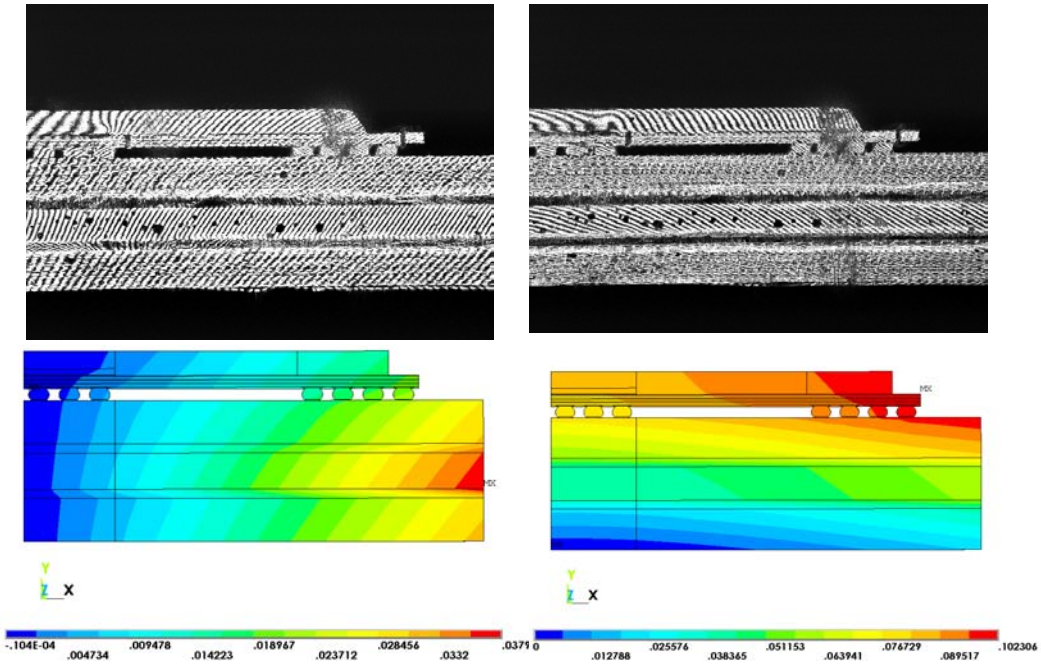


Figure 5.5 *U* and *V* field fringes at -10°C



U Field V Field

Figure 5.6 *U* and *V* field fringes at 0°C



U Field V Field

Figure 5.7 *U* and *V* field fringes at 100°C

We can see from Figure 5.4 through 5.7 that the orientation of the fringes representing regions of constant displacement coincides with the orientation of the color contours which again represents regions of constant displacement. As we move from -25°C to a stress-free temperature of 20°C, the number of fringes observed decreases. Again as we increase the temperature from the stress-free temperature to 100°C, the number of fringes observed in the package increases. The displacement in both the *U* and *V* directions was measured between the outermost solder ball and the center of the package through moiré interferometry. This displacement was compared with the displacement got from numerical analysis. Table 5.1 summarizes this comparison. The percentage error was calculated based equation 5.1.

$$\%Error = \frac{\text{Numerical result} - \text{Moire result}}{\text{Moire result}} X\,100 \qquad \text{Eq (5.1)}$$

Table 5.1 Comparison of results from moiré interferometry and numerical analysis

Temperature	Fringe Pattern	Moire interferometry (mm)	Numerical Analysis (mm)	% Error
-25°C	U	-0.014595	-0.012098	-17.1086
	V	-0.010842	-0.011728	8.17192
-10°C	U	-0.010425	-0.008064	-22.64748
	V	-0.007089	-0.007728	9.01397
0°C	U	-0.006672	-0.005376	-19.42446
	V	-0.006255	-0.005484	-12.32614
100°C	U	0.02085	0.020883	0.15827
	V	0.01668	0.015784	-5.371703

From Table 5.1, we can see that the results from moiré interferometry matches well with the results obtained from numerical analysis. It can be seen that as we move away from the reference temperature of 20°C, the average percentage error decreases. One possible reason could be the presence of

virtual reference fringes at stress free temperature whose contribution to the percent error gets reduced when the temperature of the package is far from to the reference temperature.

The fringes obtained from moiré studies can also help us to obtain knowledge about the deformation occurring in a solder ball. Figure 5.8 shows the deformation fringes in both the *U* and *V* direction at various temperatures. It can be seen that as we approach from -25°C to the reference temperature of 20°C, the number of fringes decrease. Again, as we go from the reference temperature to 100°C, the number of fringes increases.

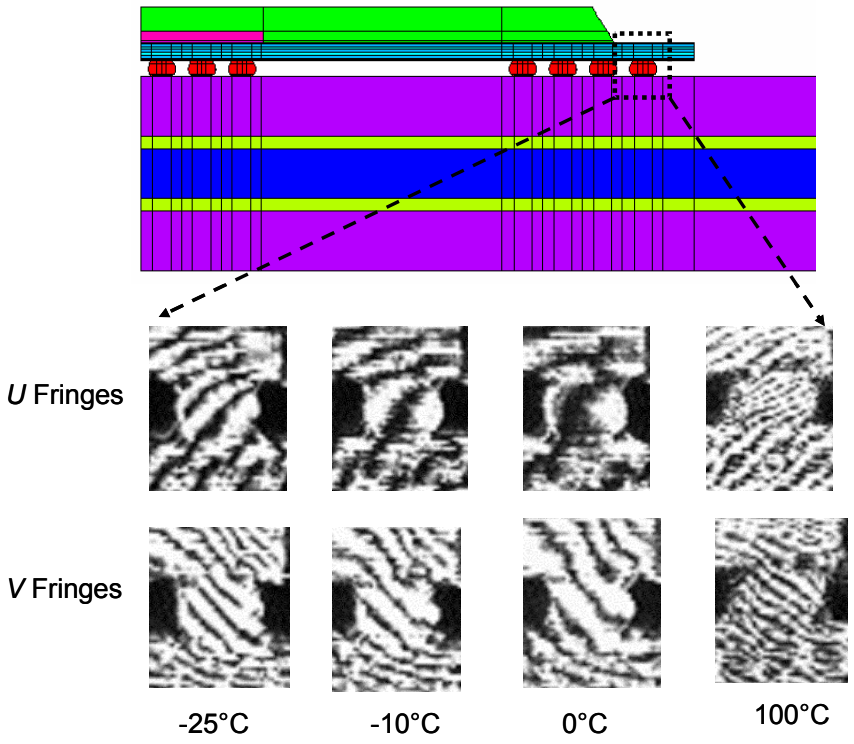


Figure 5.8 U and V fringe patters observed in a single solder ball as a function of temperature

5.1.4 Determination of material properties using moiré interferometry

Moire interferometry can be used to determine the property of materials used in a package. Determination of the in-plane CTE of FR4 was used as a

representative case. The in-plane CTE of FR4 was measured at various temperatures using moiré interferometry to verify with the CTE of FR4 assumed during simulation. The CTE of FR4 assumed during simulation was 20 ppm/K. The CTE of FR4 at various temperatures is given by equation 5.2.

$$CTE = \frac{\Delta L}{L\Delta T} = \frac{F\ X\ CI}{L\Delta T} \qquad \text{Eq (5.2)}$$

Where, ΔL is the change in length of the FR4 material along the x-axis, L is the length of the specimen along the x-axis, ΔT is the change in temperature with respect to the reference temperature of 20°C, F is the number of U fringes observed in the specimen after it has been subjected to a temperature change of ΔT and CI is the contour interval of the grating in displacement per fringe order. For the present case, the length of the specimen along the x-direction is 20 mm and the CI for the grating is 417 nm per fringe order. Table 5.2 shows the result got from moiré studies at various temperatures.

Table 5.2 CTE of FR4 at various temperatures as obtained from moiré studies

Temperature (°C)	ΔT (°C)	Number of fringes (F)	CTE (ppm/K)
-25	45	50	23.16
-10	30	34	23.63
0	20	22	22.93
100	80	72	18.76

As can be seen from Table 5.2, the CTE of FR4 is very close to the actual CTE of 20 ppm/K. The FR4 mentioned above is actually part of the package assembly and not a standalone material. Hence, the deformation of FR4 is influenced by the presence of other materials to which it is attached. The CTE obtained from moiré studies therefore differ by a little extent.

CHAPTER VI

VIRTUAL RELIABILITY ASSESSMENT OF SBGA PACKAGES

This chapter provides the details about the geometric modeling of SBGA packages. The results from the GPD model will also be discussed.

6.1 Geometric Models for the SBGA Package

The SBGA package is a laminated BT substrate with copper layer interposed between them. The copper heat spreader on top of the package serves to dissipate heat. The schematic of the package is given in Figure 6.1. The IC faces downwards and is attached to the copper heat spreader at the back. The pads at the periphery of the IC chips are wire-bonded to the copper pads on the BT substrate. The IC and the wire-bonds are encapsulated with a polymer material for protection. The copper pads on the package side and the board side are solder mask defined.

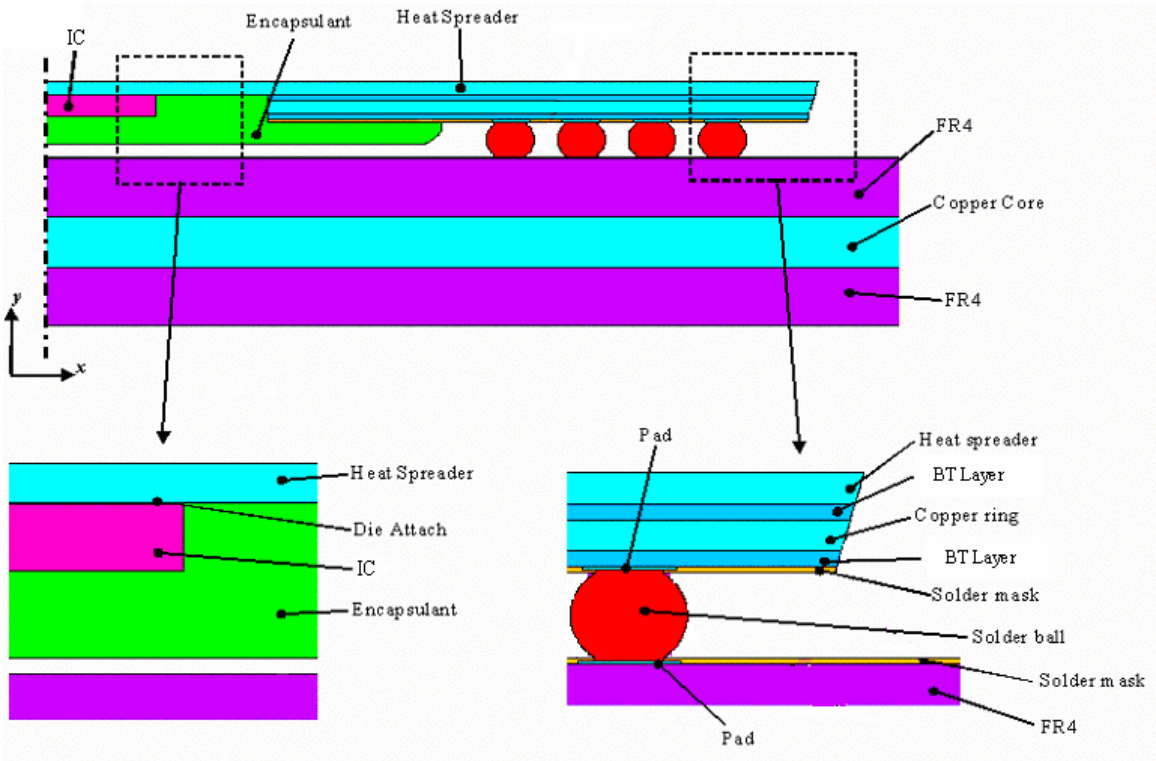


Figure 6.1 Schematic of the SBGA 352 package

Table 6.1 and 6.2 provides the dimensional details of the SBGA package. Additional details were provided by the vendor and is proprietary [Amkor, 2000].

Table 6.1 Dimensional details of the SBGA package

Package Size	35 x 35 mm
Profile Height	1.3 mm to 1.7 mm
Die Thickness	0.424 mm
Ball Pitch	1.27 mm
Ball Matrix	26 x 26 Balls
Ball Footprint	31.75 mm

Table 6.2 Thicknesses of the board layers

Board Layer	Thickness, mm
FR4	1.143
Copper Core	1.016
FR4	1.143

6.1.1 3D Generalized Plane Deformation (GPD) Model

The GPD model is a compromise between an accurate 3D model and computationally efficient 2D model. The geometry is represented by 3D elements

which are used to represent only a part of the width of the whole package. For area array packages, the model width is equal to the pitch of the package. This width would include only one solder ball in the thickness direction as shown in Figure 6.2. The geometry of the solder ball was obtained using Surface Evolver. The Surface Evolver code that was implemented to obtain the geometry is given in Appendix A. Due to the symmetry of the package, only half of the package was modeled. Hence, all the nodes on the symmetry plane were constrained in the x-direction. A single node in the bottom left-most region was constrained in all three directions to prevent rigid body motion.

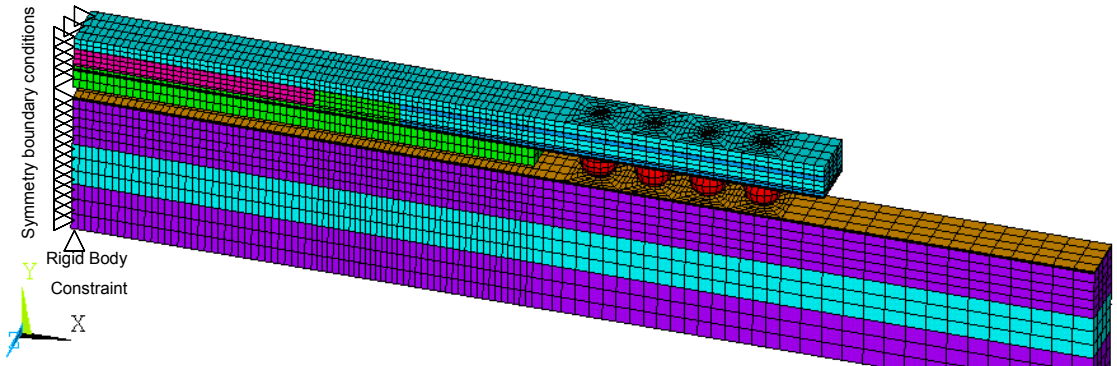


Figure 6.2 GPD model for the SBGA 352 package

The two z-faces of the strip are coupled, as shown in Figure 6.3, so that all the nodes on these two faces move together in the same direction and by the same amount.

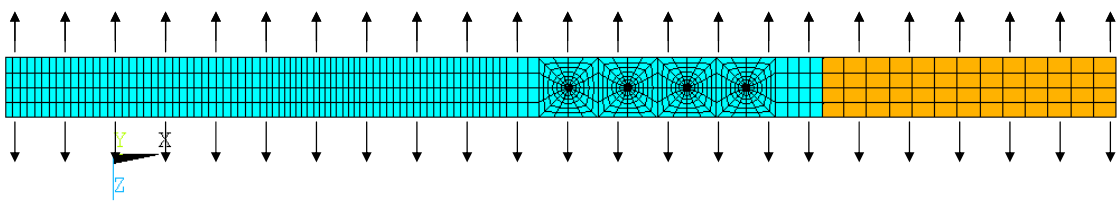


Figure 6.3 Coupled nodes in a GPD model

6.2 Material Models for the SBGA Package

Table 6.3 lists the materials that were used for modeling an SBGA package.

Table 6.3 Materials used in a SBGA package

Part Name	Material
Dielectric	Bismaleimide-Triazine (BT)
Heat Spreader and Ring	Copper
Plating Mask	Bismaleimide-Triazine (BT)
Solder Mask	Epoxy
Solder Balls	62Sn/36Pb/2Ag solder
Encapsulation	Epoxy
Die Attach Material	Silver Filled Epoxy
Die	Silicon
Board	FR4 with Copper Core

The material properties for copper, BT, silicon, encapsulant and die-attach were obtained from the data sheets provided by the manufacturer. Table 6.4 lists the material properties of these three materials.

Table 6.4 Linear elastic material properties for SBGA package[Amkor, 2000]

Material	Copper	BT	Silicon	Encapsulant	Die Attach
Property	Value	Value	Value	Value	Value
E, MPa	1.21×10^{5}	1.86×10^{5}	1.60×10^{5}	8.96×10^{3}	2.62×10^{3}
ν	0.35	0.36	0.23	0.35	0.42
G, MPa	4.48×10^{4}	6.84×10^{4}	6.50×10^{4}	3.30×10^{3}	922×10^{2}
α_x (10^{-6}/°C)	16	16.7	2.6	19	160
α_z (10^{-6}/°C)	isotropic	16.7	isotropic	isotropic	isotropic
α_y (10^{-6}/°C)		57			

Copper, silicon, encapsulant and die-attach were modeled using temperature independent linear elastic properties. The CTE of BT is modeled as being temperature independent orthotropic and its mechanical properties are modeled using temperature independent linear elastic properties.

The FR4 used in the PCB is modeled as being temperature dependent orthotropic and linear elastic. Table 6.5 lists the material properties of FR4 that was used for modeling.

Table 6.5 Material properties of FR4 [Barker and Dasgupta, 1993, Michaelides, 1999]

T, °C	30	95	110	125	150	270
E_x (MPa)	22400	20680	19970	19300	17920	16000
E_z (MPa)	22400	20680	19970	19300	17920	16000
E_y (MPa)	1600	1200	1100	1000	600	450
ν_{xz}	0.136	0.136	0.136	0.136	0.136	0.136
ν_{xy}	0.1425	0.1425	0.1425	0.1425	0.1425	0.1425
ν_{yz}	0.1425	0.1425	0.1425	0.1425	0.1425	0.1425
G_{xz} (MPa)	630	600	550	500	450	441
G_{xy} (MPa)	199	189	173	157	142	139.3
G_{yz} (MPa)	199	189	173	157	142	139.3
α_x (10^{-6}/°C)	20	20	20	20	20	20
α_z (10^{-6}/°C)	20	20	20	20	20	20
α_y (10^{-6}/°C)	86.5	86.5	243	400	400	400

The solder mask was modeled as being temperature dependent isotropic with linear elastic properties [Schubert et al, 1997]. Table 6.6 lists the material properties of the solder mask that was used for modeling.

Table 6.6 Material properties for solder mask material [Cindas, 1995]

T, °C	-55	22	70	100	150
E, MPa	6000	4100	1420	330	100
ν	0.34	0.38	0.45	0.49	0.49
α_x (10^{-6}/°C)	36	36	36	36	36
α_z (10^{-6}/°C)	isotropic				
α_y (10^{-6}/°C)					

6.2.1 Solder Material Models

The deformation behavior of the solder material is highly rate dependent. The rate dependency is taken into account by modeling the solder material using elastic-plastic-creep material model.

The elastic-plastic-creep model for 62Sn/36Pb/2Ag solder uses a temperature dependent model with separate equations representing the rate dependent and rate independent deformation behavior. The rate independent behavior is represented by equation 6.1.

$$\gamma_p = C_2\left(\frac{\tau}{G(T)}\right)^m \qquad \text{Eq. (6.1)}$$

Where $G(T)=G_o-G_1T$ is the shear modulus of the solder material. The constants for equation 6.1 along with G_o and G_1 are shown in Table 6.7 [Darveaux and Banerji, 1992]. The CTE and poisson's ratio of the material was assumed to be 24.5x10^{-6}/K and 0.35 respectively.

Table 6.7 Constants for the elasto-plastic model

C_2	m	G_o, 10^6 psi	G_1,10^3 psi
6.6×10^7	3.5	1.9	8.1
		G_o, MPa	G_1, MPa
		1.3×10^4	56

Assuming a von Mises yield criteria, the relations given in equations 6.2 and 6.3 can be derived.

$$\sigma = \tau\sqrt{3} \qquad \text{Eq. (6.2)}$$

$$\varepsilon = \frac{\gamma}{\sqrt{3}} \qquad \text{Eq. (6.3)}$$

Using the constants given in Table 6.6 in conjunction with equations 6.2 and 6.3, a stress-strain plot to model the time-independent behavior can be obtained as shown in Figure 6.4. Solder joints are known to exhibit Bauschinger effect [Wang et al, 2001]. Hence, the plasticity given in Figure 6.4 was modeled using kinematic hardening.

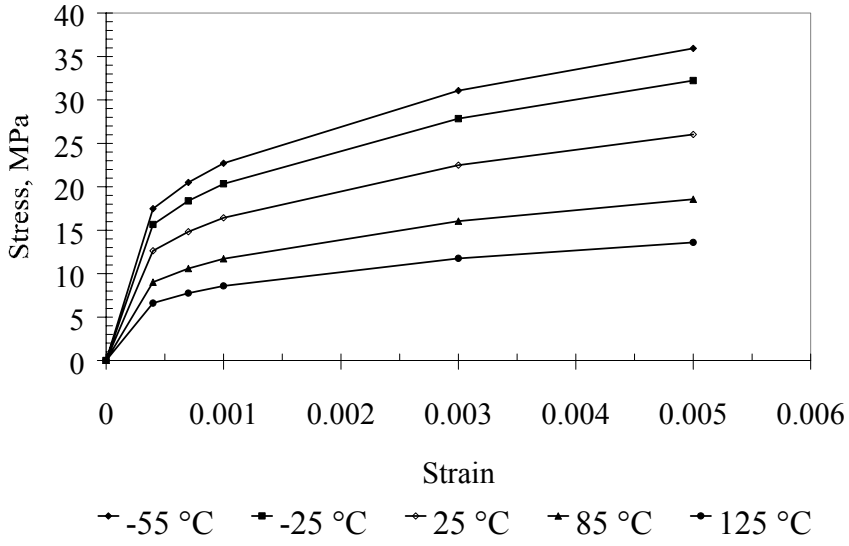


Figure 6.4 Stress-strain plot for rate-independent behavior

The creep occurring in the solder joint can be classified as primary, secondary and tertiary creep. The primary and tertiary creep durations are quite small when compared to secondary creep. Hence, only secondary creep is modeled for this work. The secondary creep equation is available in the literature in Garafalo form as shown in equation 6.4. The constants for this equation are given in Table 6.8 [Darveaux and Banerji, 1992].

$$\dot{\gamma}_s = C_1 \frac{G(T)}{T}\left[\sinh\left(\alpha \frac{\tau}{G(T)}\right)\right]^n \cdot \exp\left(\frac{-Q}{kT}\right) \qquad \text{Eq. (6.4)}$$

Table 6.8 Constants for the Garafalo equation

C_1, $K\cdot sec^{-1}psi^{-1}$	α	n	Q, eve	k
0.0989	1300	3.3	0.548	8.62×10^{-5}
C_1, $K\cdot sec^{-1}MPa^{-1}$				
14.34				

The Garafalo form of secondary creep equation, given in equation 6.4, cannot be directly represented in ANSYS 7.0 along with kinematic hardening which is shown in Figure 6.4. However, regression can be used to fit a power law

equation to the data generated by equation 6.4. The power law form of creep can be easily implemented with kinematic hardening using ANSYS 7.0. Equation 6.5 shows the power law equation and Table 6.9 shows the constants used for equation 6.5 [Pyland, 2002].

$$\dot{\varepsilon}_s = A\sigma^n e^{-(Q/R_g T)} \qquad \text{Eq. (6.5)}$$

Table 6.9 Constants for the power law equation

Constant	Value
A	9.10×10^{-3} $(MPa)^{-n}$ $(s)^{-1}$
n	7.67
Q	79.4 kJ/mol
R	8.314×10^{-3} kJ/mol-K

6.3 Thermo-mechanical Analysis of SBGA Package

The SBGA package was simulated with MIL-STD-883E-condition B thermal cycling conditions with a stress free temperature of 183°C. The MIL-STD 883E-condition B is a one hour thermal cycle between -55°C to 125°C with 20 minute dwell at each temperature and a 10 minute ramp time between each temperature. Figure 6.5 shows the thermal profile that the packages were simulated with.

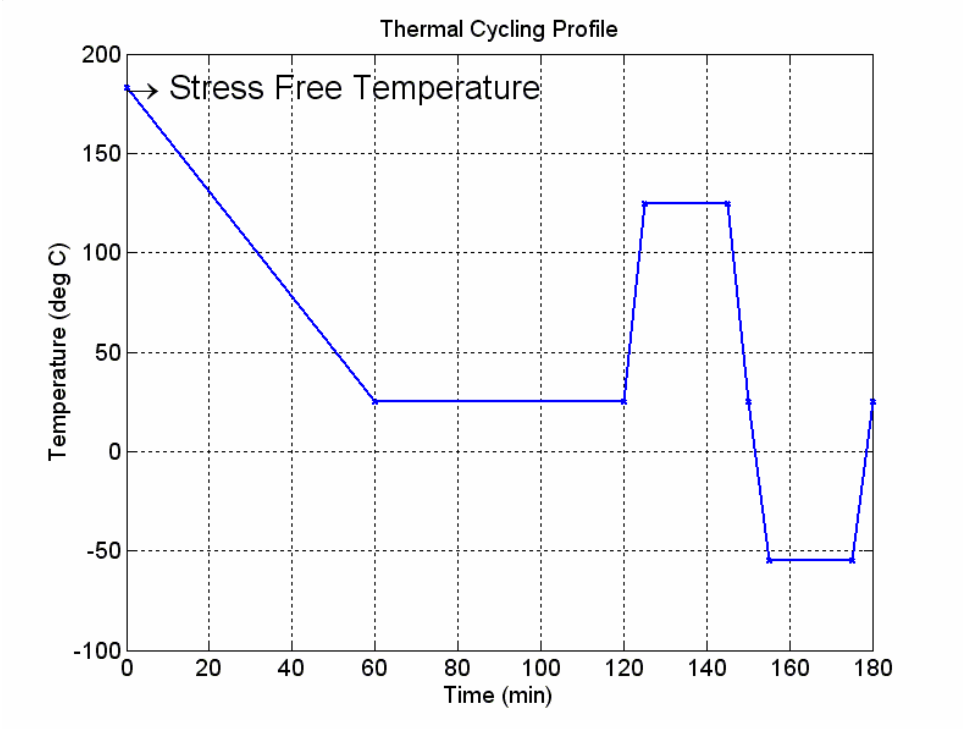


Figure 6.5 MIL-STD-883E thermal profile

When the package is subjected to a change in temperature, the CTE mismatch between the package and the board causes solder joint fatigue. For the SBGA package, this differential expansion is less because the CTE difference between the package and the board is low. Accumulated inelastic work was used as a metric to determine solder joint fatigue. As was done for the PBGA package, the SBGA package was also subjected to several thermal cycles till stabilized results were obtained from each thermal cycle. Figure 6.6 shows the contours of the inelastic work accumulated in the four solder balls.

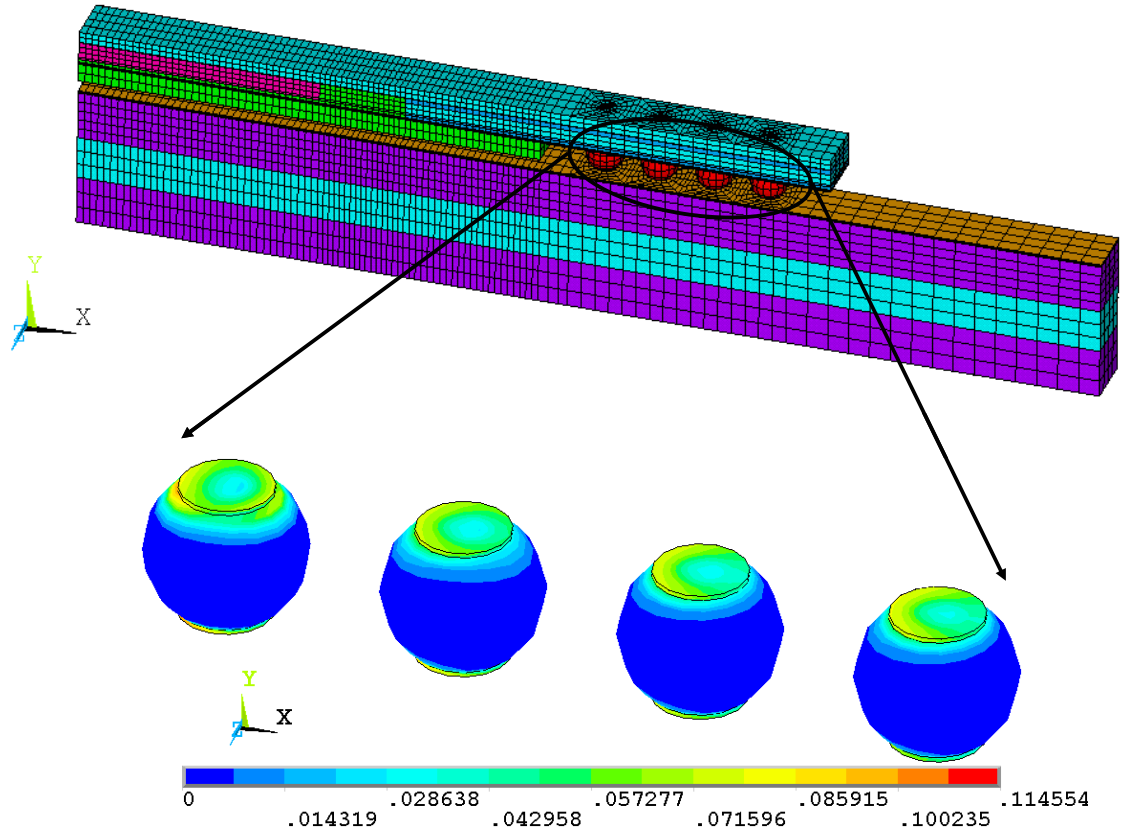


Figure 6.6 Accumulated inelastic work contours for the SBGA 352 package

Very little variation of the accumulated inelastic work with displacement was observed. The inelastic work was also found to be of the same order for all the four solder joints at both the package side and the board side. However, the inelastic work accumulation in the solder joints at the package side was found to be slightly higher than that at the board side. Cross-sections taken from the actual thermal cycled samples revealed that the solder joint failure due to crack propagation occurred mostly at the package side.

Volume averaging was used to find the average accumulated inelastic energy density at the package side. Figure 6.7 shows the four strips corresponding to the four solder balls at which the volume averaging was done.

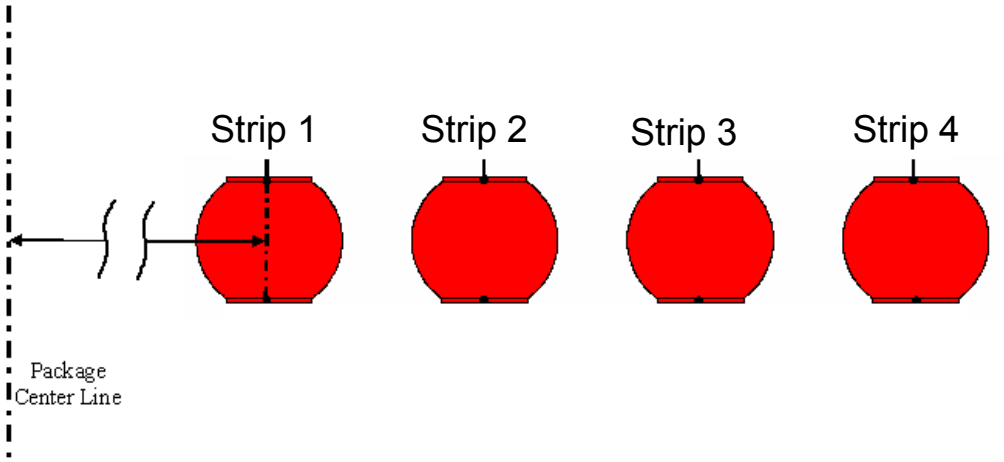


Figure 6.7 Strips for volume averaging of accumulated work

Table 6.10 shows the volume averaged accumulated inelastic energy density at each of these four strips found by numerical analysis. It can be noted from Table 6.10 that the inelastic energy accumulation is almost similar for all the four solder joints. Though the highest accumulation of inelastic energy density occurs at the outermost solder joint, one could expect any of the four solder joints to fail early.

Table 6.10 Accumulated inelastic energy density

Strip Number	Accumulated inelastic energy density per cycle (N/mm^2)
1	0.0629
2	0.0598
3	0.0622
4	0.0661

The results from Table 6.10 can be used in conjunction with equation 6.6, 6.7, 6.8 and 6.9 to obtain the number of cycles for crack initiation and to obtain the variation of crack length with number of cycles.

$$N_o = K_1 \Delta W_{ave,acc}^{\ K_2} \qquad \text{Eq (6.6)}$$

$$\frac{dx}{dN} = K_3 \Delta W_{ave,acc}^{\ K_4} \qquad \text{Eq (6.7)}$$

$$N_p(x) = \frac{x}{da/dN} \qquad \text{Eq (6.8)}$$

$$N(x) = N_o + N_p(x) \qquad \text{Eq (6.9)}$$

where, x is the length of the crack in the solder as shown in Figure 6.8. Table 6.11 shows the constants that were used for equation 6.6 and 6.7.

Table 6.11 Constants for the Darveaux model

Constant	Value
K_1	10.5208
K_2	-1.52
K_3	0.00211356
K_4	0.99

The variation of the cracked solder ball area as a function of number of cycles can be determined. Figure 6.9 illustrates this dependency for all four strips.

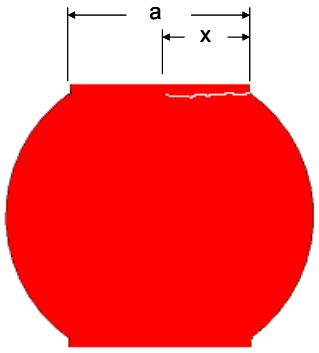


Figure 6.8 Schematic of a cracked solder ball.

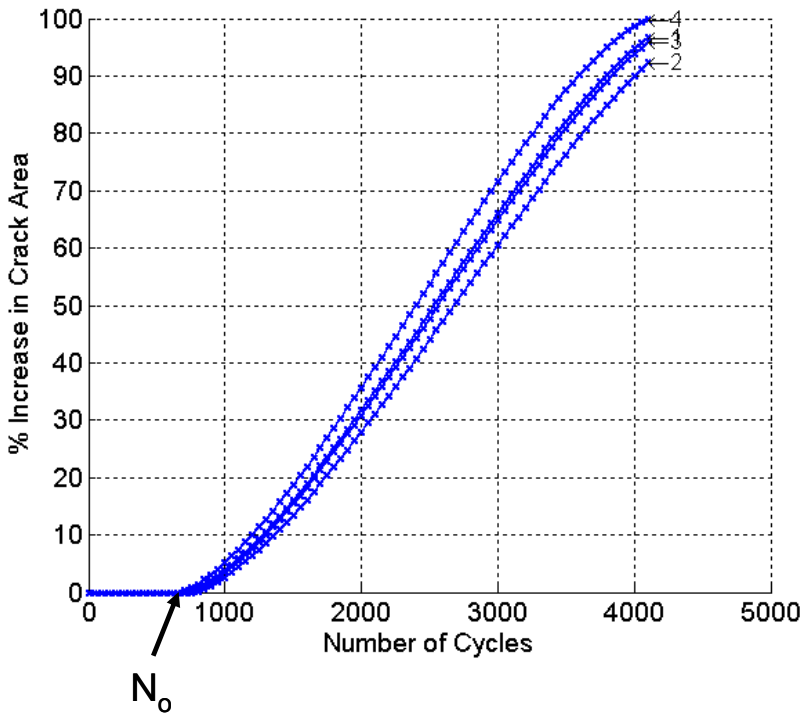


Figure 6.9 Variation of cracked area as a function of number of cycles

We can see that since the ΔW for all the four strips are approximately same, the crack begins to originate at around the same number of cycles.

6.4 Electrostatic Model for Solder Ball Resistance

An electrostatic analysis can be performed to find the change in the resistance of a single solder ball as a function of its cracked area. The methodology has been outlined in section 2.8.1. As outlined in section 2.8.1, it is necessary to find the change in resistance of the solder ball as it cracks. The solder balls are connected in series to form a daisy chain. It is hence enough to find the correlation between crack length and resistance change for one solder ball. Figure 6.10 shows a typical solder ball with the copper pads that would form part of a daisy chain.

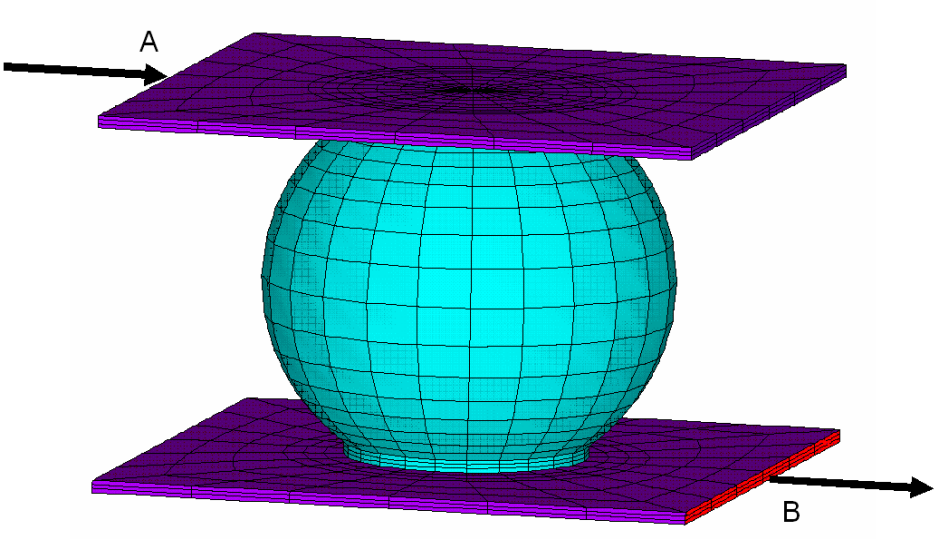


Figure 6.10 Current flow through a solder ball

Surfaces *A* and *B* were maintained at 1 volt and 0 volt respectively. All other surfaces were electrically insulated so that current does not pass through them. As a result, the current would flow from surface *A* to surface *B* through the solder ball. A measure of the current that flows at either of these surfaces in combination with the applied voltage would give us the resistance of the solder ball. Crack can then be simulated by selectively deleting elements near the solder ball fillet. This would cause the current flow and the resistance of the solder ball to change. A correlation can then be obtained between the cracked area and the resistance of the solder ball. Figure 6.11 shows a plot of this variation.

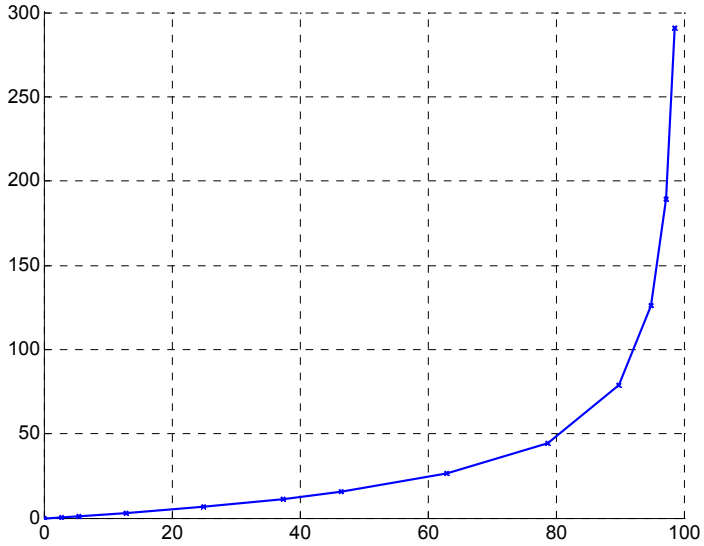


Figure 6.11 % increase in cracked area vs. % increase in resistance of solder ball

Combining the results from Figure 6.9 and 6.11, the change in resistance of each individual solder ball as a function of number of cycles can be determined. This is shown in Figure 6.12.

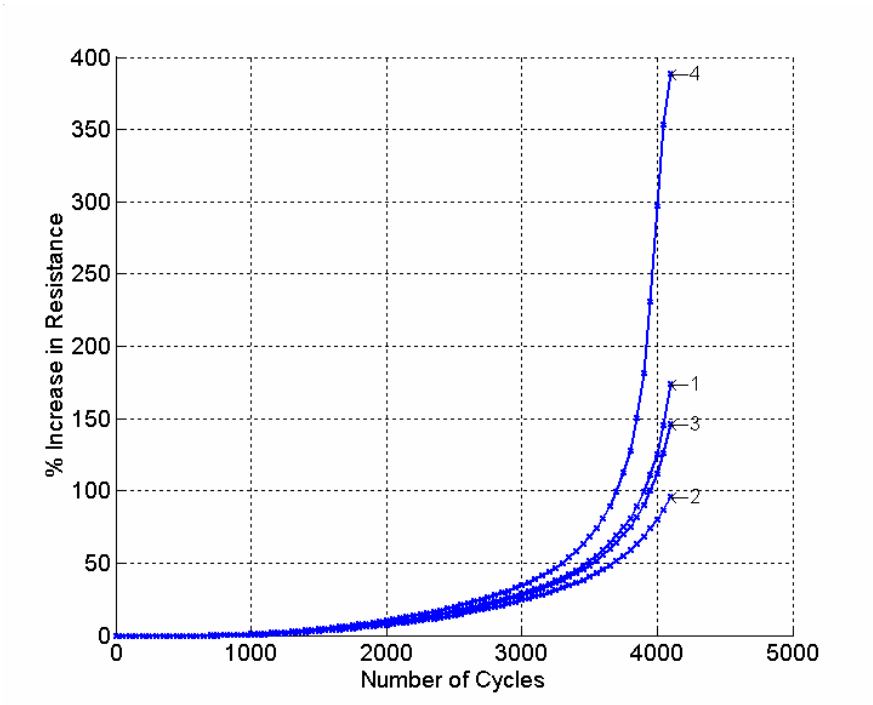


Figure 6.12 Variation of individual solder ball resistance with number of cycles

The resistance of each of the solder ball can now be added with each other to determine the resistance of the daisy chain consisting of the four solder balls. Figure 6.13 shows the variation of the daisy chain resistance with number of cycles.

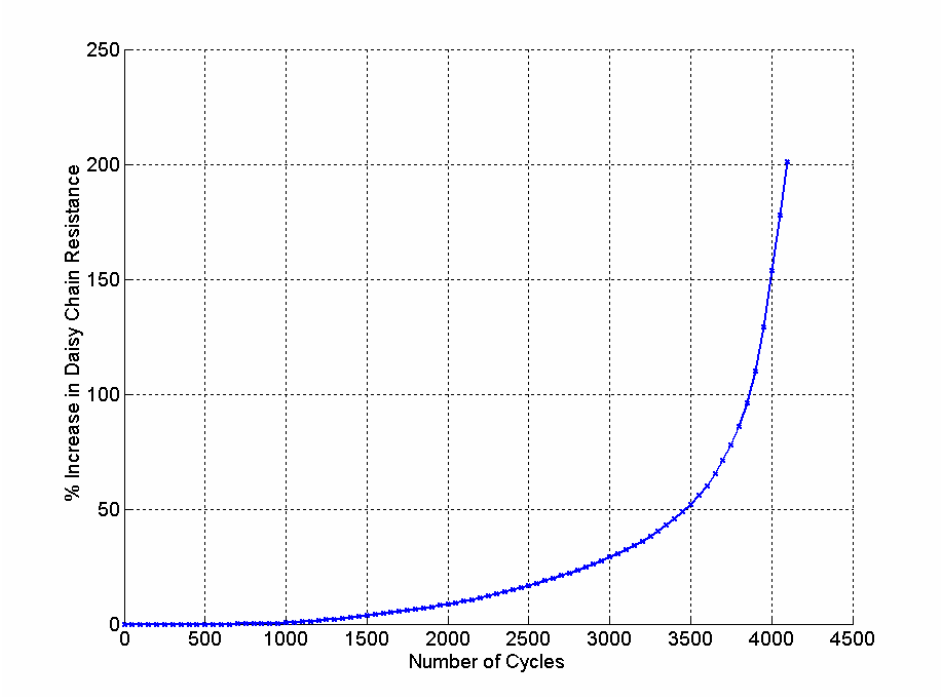


Figure 6.13 Variation of daisy chain resistance with number of cycles

From Figure 6.13 it can be seen that the mean number of cycles for 100% change in resistance is about 3830 cycles. It should be pointed out that in the actual package, the daisy chain consisted of all the 352 solder balls. In this GPD model however, the daisy chain consists of only four solder balls. The package can be thought of as being composed of various GPD models placed by the side of each other. And it was assumed that the collective representation of the strains in the whole package can be represented by the strains occurring in the four solder joints.

CHAPTER VII

EXPERIMENTAL VALIDATION OF VIRTUAL RELIABILITY ASSESSMENT MODELS OF SBGA PACKAGES

This chapter provides experimental details of accelerated thermal cycling of SBGA packages and the validation of numerical models with experimental data.

7.1 SBGA Test Vehicle Description

Figure 7.1 shows the test vehicle 1 (TV1) with the SBGA assembled on it. In addition to SBGA package, CI-CGA packages were also assembled on the board. The channel numbers are marked on the package.

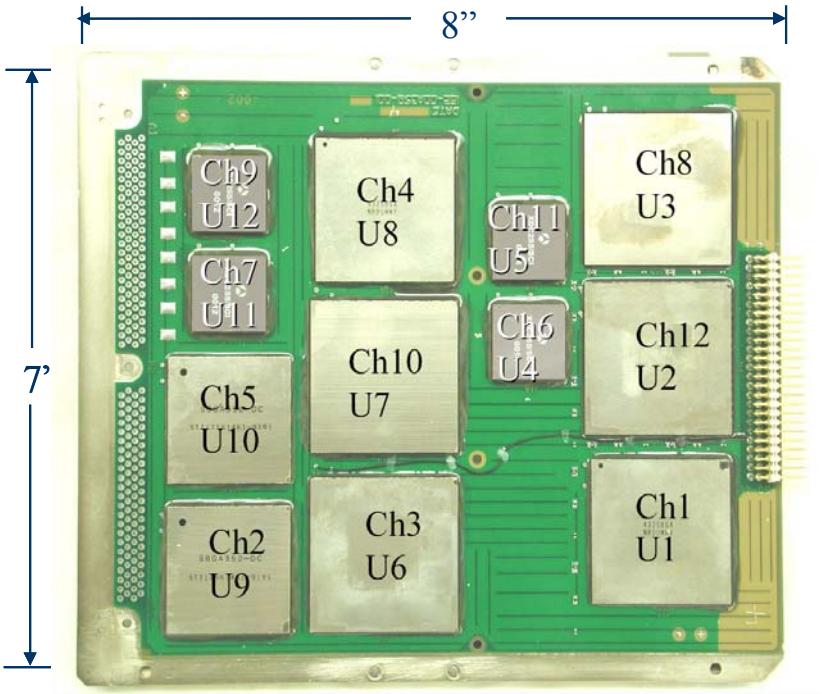


Figure 7.1 SBGA test vehicle

Table 7.1 shows the component designators, package types and their outline dimensions. The packages were assembled on a three layered PCB. The board consists of two layers of FR4 with a copper core sandwiched between these two layers. The copper core provides rigidity to the board and also serves as a heat spreader.

Table 7.1 Package designations and dimensions

Locator	Type	Package size*, mm
Ch1	432 SBGA	40
Ch12	560 SBGA	42.5
Ch8	560 SBGA	42.5
Ch6	255 CI-CGA	21
Ch11	255 CI-CGA	21
Ch3	560 SBGA	42.5
Ch10	560 SBGA	42.5
Ch4	432 SBGA	40
Ch2	352 SBGA	35
Ch5	352 SBGA	35
Ch7	255 CI-CGA	21
Ch9	255 CI-CGA	21

*all packages are square

7.2 Experimental Setup and Results

Each test vehicle has two SBGA 352 packages assembled on it and two such test vehicles were subjected to thermal cycling in a thermal chamber using MIL-STD 883E - condition B thermal cycling. The thermal cycling involves cycling between -55°C to 125°C with a dwell time of 20 minutes at either temperature and a ramp time of 10 minutes (ramp rate of 18°C/min) between these two temperatures. Figure 7.2 shows the thermal chamber at Georgia Tech in which the thermal cycling was performed.

Figure 7.2 Thermal chamber for accelerated thermal cycling

All the solder joints in the SBGA package were daisy chained. Figure 7.3 shows the ball side view of the daisy chain. When connected to the board side part of the daisy chain, a single continuous daisy chain is formed as shown in Figure 7.4. The resistance of this daisy chain was monitored in-situ during thermal cycling. A 100% increase in the resistance of the daisy chain was used as a criterion to determine the failure of the package. The cumulative failure of the packages during thermal cycling was recorded.

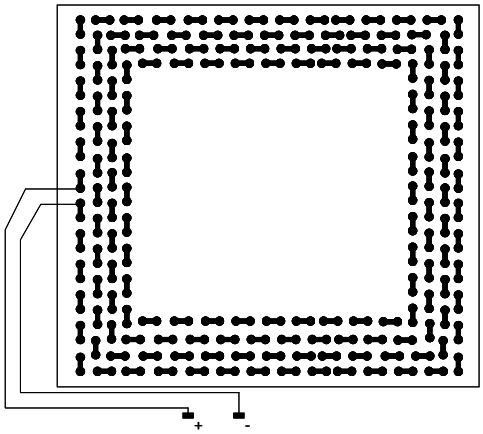


Figure 7.3 Ball side view of the daisy chain

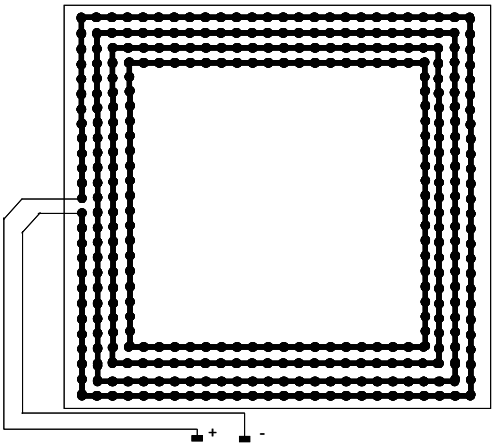


Figure 7.4 Continuous daisy chain

The data acquisition was done using LabView 6.0. A schematic of the data acquisition system is shown in Figure 7.5.

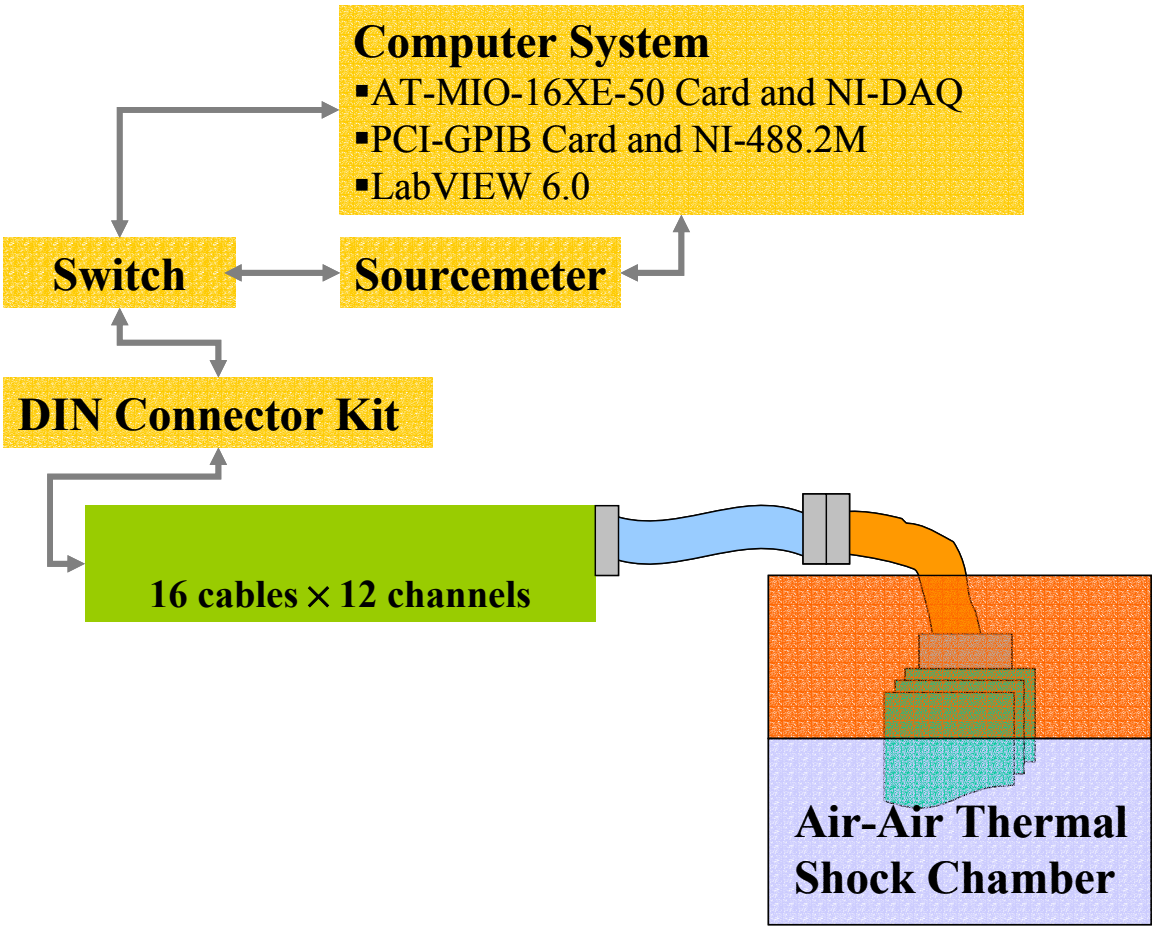


Figure 7.5 Schematic of the data acquisition system

The daisy chain electrical resistance in the air-to-air thermal chamber was monitored in-situ. Each PWB board had twelve channels corresponding to twelve packages mounted on it. The resistance of a single board was captured using one cable consisting of at least 12 channels. Data acquisition card by National Instruments was then used to obtain the actual resistance of each of the channels in each of the cables. LabView 6.0 software was then used to communicate between the data acquisition card and the user.

Figure 7.6 shows the plot of cumulative failure percentile as a function of number of cycles as found by the experiments performed at Georgia Tech. The mean cycles to failure found from Georgia Tech experimental data was found to be 3462 cycles.

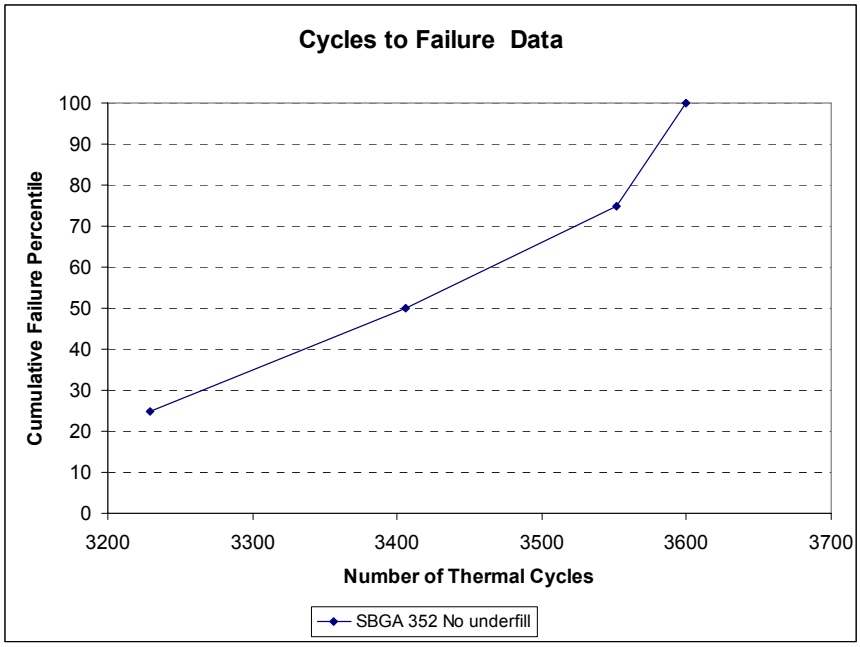


Figure 7.6 Cumulative failure percentile for SBGA packages (Georgia Tech data)

ITRI [Interconnection Technology Research Institute, 1998] has performed thermal cycling tests on SBGA 352 packages and has published reliability data

for their failure during accelerated thermal cycling. The temperature range for the tests was from -55°C to 125°C. The actual temperature ramp rates were measured during thermal cycling and were found to vary from 10°C/min to 15°C/min with an average of 12.9°C/min. Figure 7.7 shows the thermal profile measured in-situ during testing.

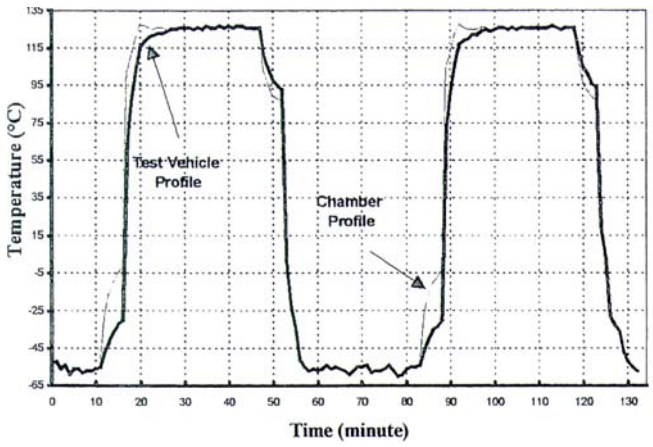


Figure 7.7 Thermal profile for ITRI thermal cycling

Figure 7.8 shows the plot of cumulative failure percentile as a function of number of cycles as found by ITRI. The mean number of cycles to failure was found to be 3300 cycles.

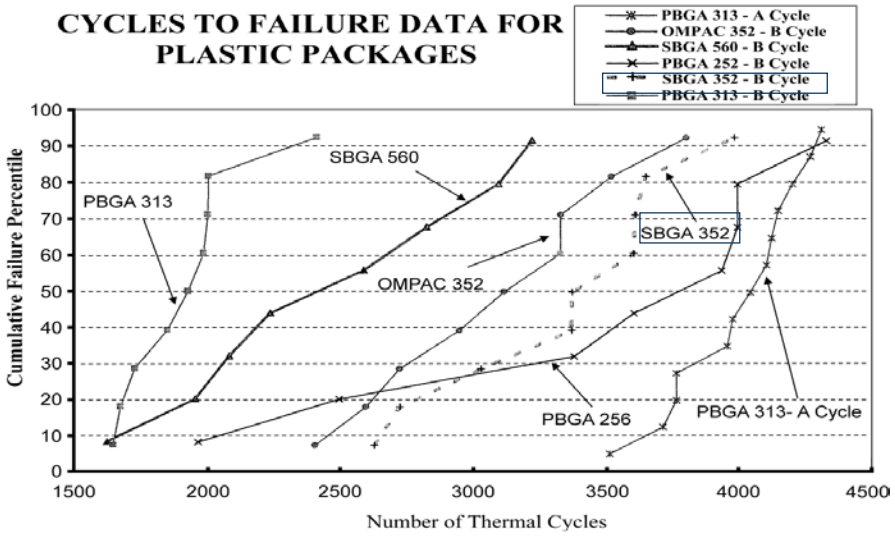


Figure 7.8 Cumulative failure percentile for SBGA packages (ITRI data)

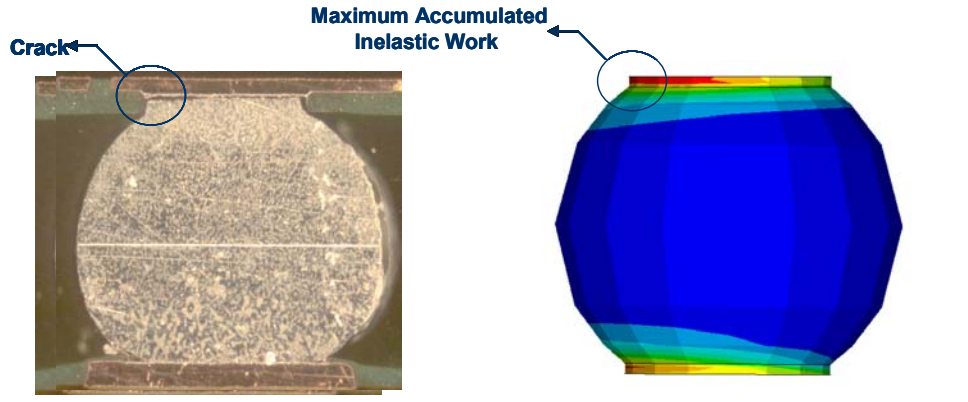
7.3 Model Validation Using Thermal Cycling

Model validation involves comparing the results from numerical analysis with experiments. Section 6.4 outlined the results from numerical simulation. Results from the ATC tests conducted at Georgia Tech and at ITRI matches well with the results obtained by numerical simulation. Table 7.2 summarizes this result.

Table 7.2 Summary of thermal cycling results

	Method	Mean number of cycles to failure
Thermal Cycling at Georgia Tech	Experimental	3462
ITRI	Experimental	3300
Numerical analysis	Simulation	3830

Cross-sections were performed on the failed SBGA 352 packages to assess the location of the crack growth in the solder joint. Figure 7.9a shows the cross section of the outermost solder ball in the SBGA package. The location of the crack growth matches well with the location of the maximum accumulated plastic work got by simulation as shown in Figure 7.9b.



a. Cross-section of outermost solder ball b. Accumulated inelastic work from simulation

Figure 7.9 Comparison between cross-sectioning and FEA analysis

7.4 Model Validation Using Moire Interferometry

In addition to thermal cycling, deformation studies using moiré interferometry studies were performed on the SBGA package. This provides a direct means to validate the model based on the actual deformation occurring in the solder ball at the microscopic level. The theory behind the working of moiré interferometry has been explained in section 2.8.2. The modeling and experimental details will be provided next.

7.4.1 Experimental Details and Geometric Models for Moire Interferometry

The SBGA package was cut along the centerline to include 3 rows of solder balls. The cut sample was then polished through the rows of solder ball to expose the cut surface. A grating was applied on the polished surface and the sample was subjected to thermal loading to monitor the strains and displacements in the package cross-section. Details regarding the sample preparation and the thermal loading are similar to ones used for PBGA package.

A geometric model was constructed to match the geometry of the cut sample. Figure 7.10 shows the geometry of the sample that was used for the modeling purpose.

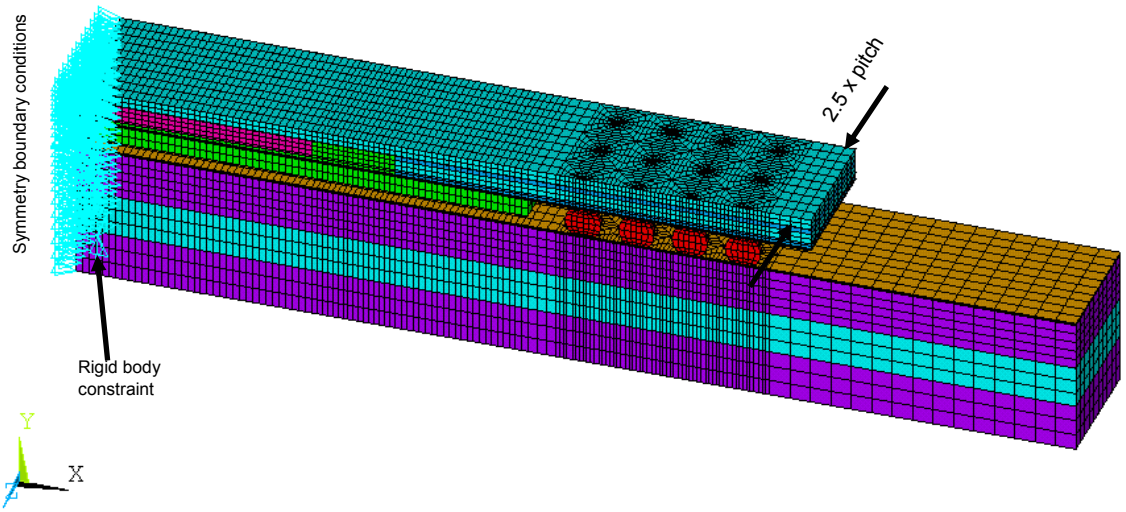


Figure 7.10 SBGA sample used for moiré interferometry

The boundary conditions include the symmetry boundary condition of constraining all the nodes on the left-most surface in the *X*-direction and constraining one node along the left-most edge of the package in all three directions to prevent rigid body motion.

7.4.2 Comparison of Results from Moire Interferometry and Geometric Modeling

Since the grating was applied to the sample at room temperature, a stress-free temperature of 20°C was assumed for simulation purposes. Figure 7.11 and 7.12 show the virtual reference fringe grating at 20°C for the *U* field and *V* field respectively.

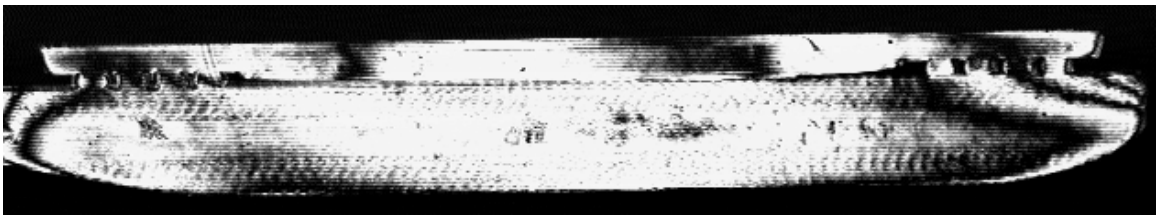


Figure 7.11 *U* field virtual reference grating

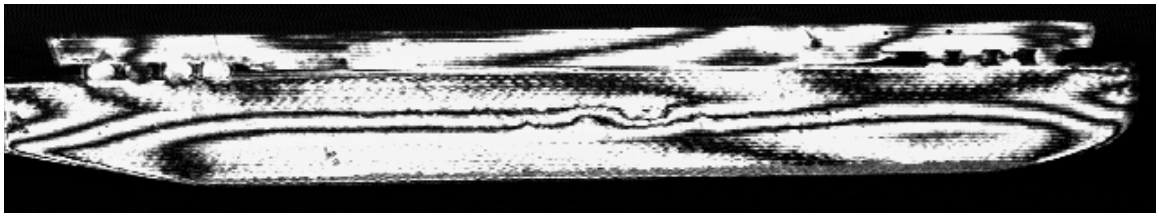


Figure 7.12 *V* field virtual reference grating

It can be observed from Figure 7.11 and 7.12 that there are finite number of fringes in both the *U* and *V* directions, even at reference temperature. These fringes are due to the presence of strains in the sample during its removal from the grating. The number of reference fringes in the *V* direction slightly is higher than that of *U* direction. This indicates that, removal of the sample from the grating, induced more strain in the *V* direction than *U* direction.

The fringe patterns in the sample were measured at -50°C and 100°C. Figure 7.13 and 7.14 show the fringe patterns in the *U* and *V* directions observed using moiré interferometry at -50°C along with the contour plot of the displacement fringes obtained from numerical analysis. The grating that was used had a frequency of 1200 lines/mm. This would correspond to a distance of 417 nm per fringe order. The numerical results obtained from simulation were plotted as an isosurface plot of the displacements in the *U* and *V* directions. The contour interval of these iso-surfaces was adjusted to 417 nm.

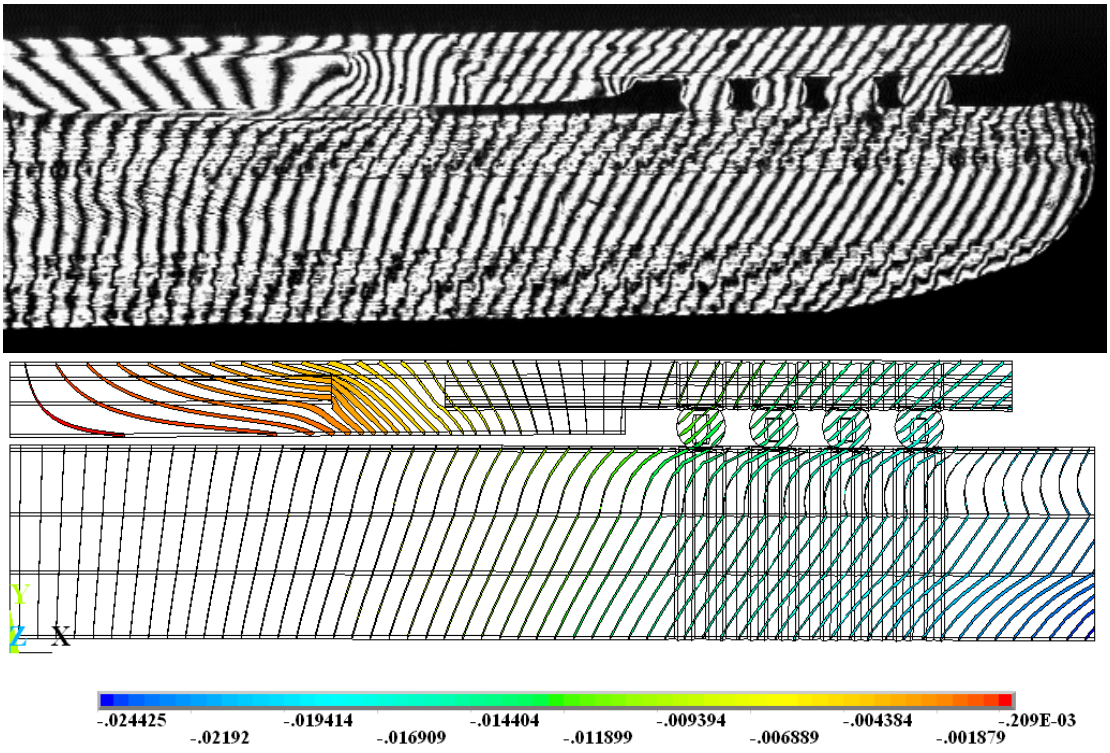


Figure 7.13 *U* field fringes at -50°C

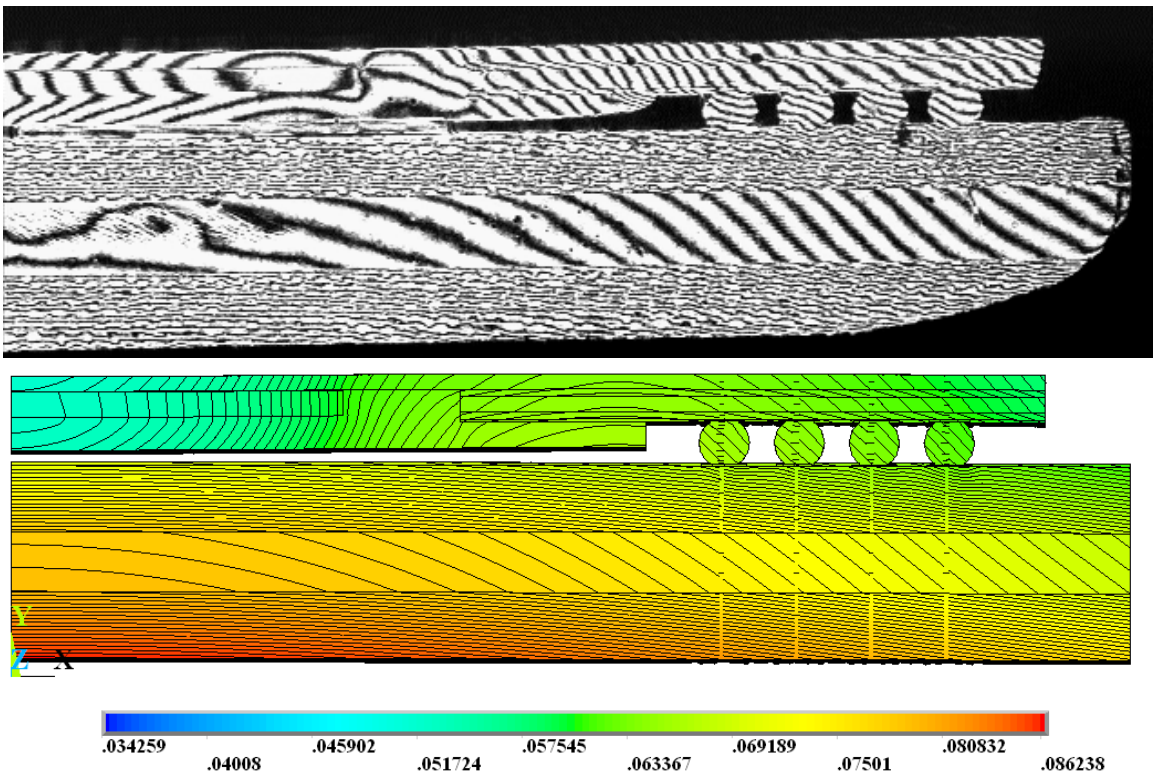


Figure 7.14 *V* field fringes at -50°C

We can see from Figures 7.13 and 7.14 that the orientation and the number of the fringes predicted by the numerical simulation agree well with the orientation and the number of fringes measured using laser moiré. This validates the overall methodology employed in the model. In Figure 7.14, however, the *V* directional fringes near the IC region do not agree between the simulated results and experimental data. This disagreement is possibly due to presence of significant number of *V* fringes in the reference state as shown in Figure 7.12.

Figure 7.15 and 7.16 show the fringe patterns in the *U* and *V* directions observed using moiré interferometry at 100°C along with the contour plot of the displacement fringes obtained from numerical analysis. The distance between the fringes obtained from moiré interferometry for the *U* and *V* field was 417 nm. For the plots obtained from simulation, the contour interval for the fringes in the *U* direction was 417 nm. The contour interval for fringes in the *V* direction was 518 nm. This is because ANSYS can represent only 128 constant displacement contours. If the actual displacement of the package exceeds (417 x 128)nm, then it is not possible to maintain a contour interval of 417 nm in the simulation plots.

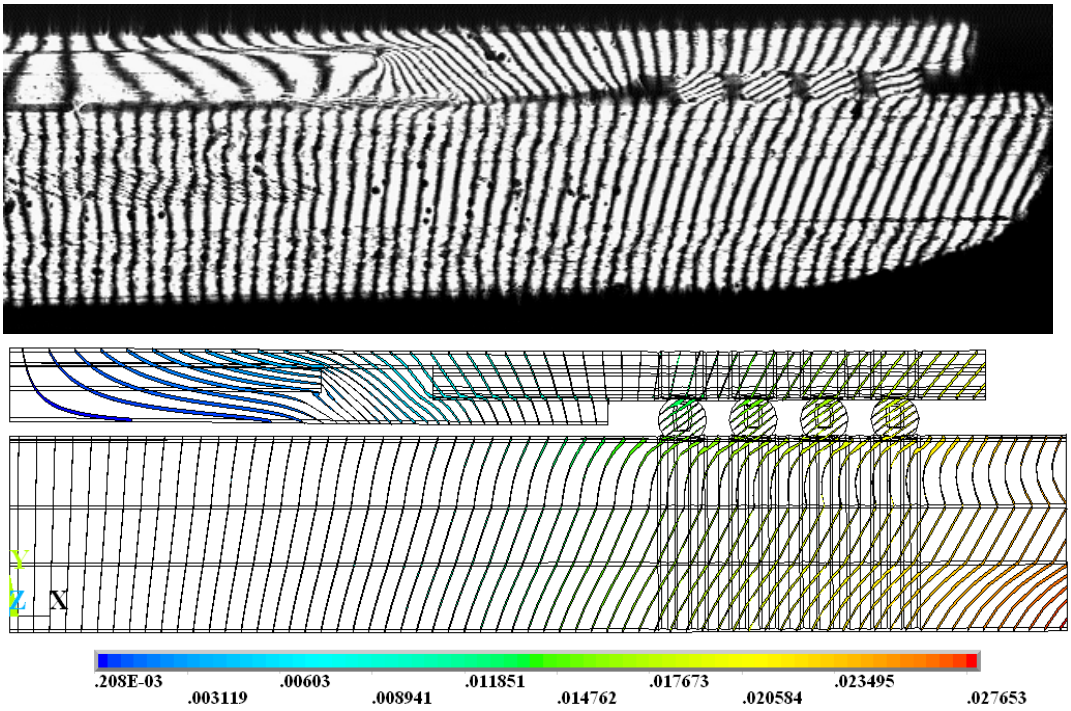


Figure 7.15 *U* field fringes at 100°C

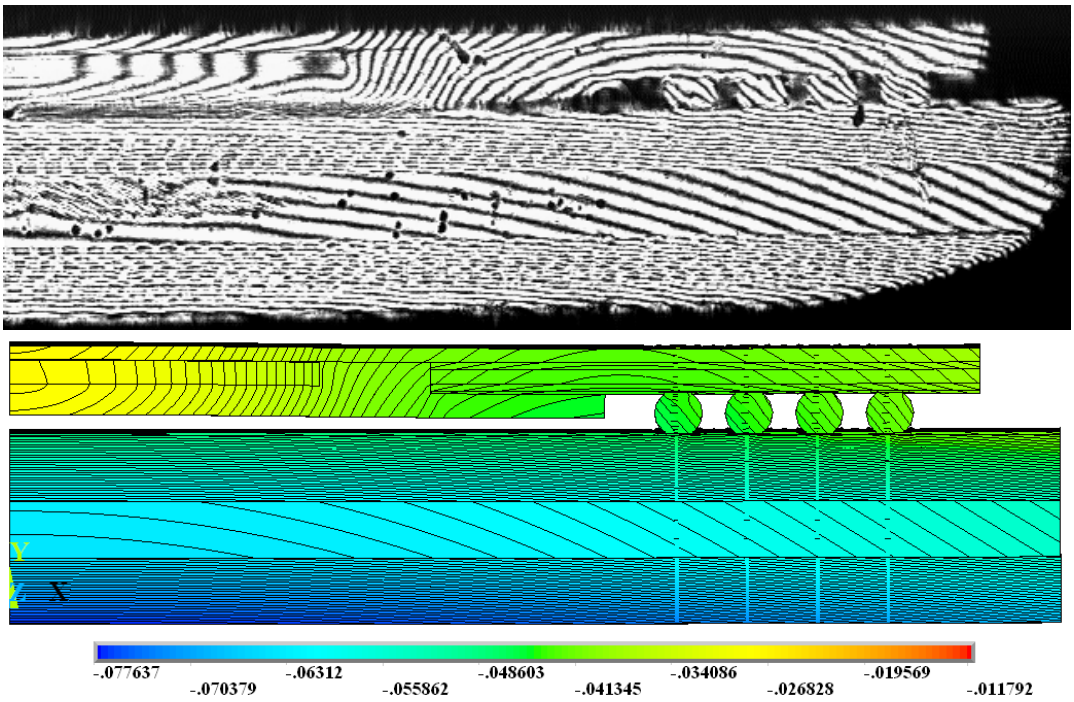


Figure 7.16 *V* field fringes at 100°C

We can see from Figure 7.15 and 7.16 that the orientation and the number of fringes in the assembly obtained from numerical simulation match well with the orientation and the number of fringes obtained from moiré interferometry. Numerical analysis also captures the slight curvature of the *V* field fringes in the region above the inner most solder.

The displacement in both *U* and *V* directions was measured between the outermost solder ball and the center of the package through moiré interferometry. This displacement was compared with the displacement got from numerical analysis. Table 7.3 summarizes this comparison. The percentage error was calculated based on equation 7.1.

$$\%Error = \frac{\text{Numerical result} - \text{Moire result}}{\text{Moire result}} X\,100 \qquad \text{Eq. (7.1)}$$

Table 7.3 Comparison of results from moiré interferometry and numerical analysis

Temperature	Fringe Pattern	Moire interferometry (mm)	Numerical analysis (mm)	% Error
-55 °C	U	-0.017097	-0.017514	2.43%
	V	0.007506	0.009174	22.22%
100 °C	U	0.018348	0.019182	4.54%
	V	-0.007923	-0.00935	18.01%

We can observe from Table 7.3 that the results from numerical analysis match well with the results obtained from moiré interferometry. At both -55°C and 100°C, the *U* displacements obtained from numerical analysis match well with the *U* displacements obtained from moiré interferometry. The percentage error in the *V* displacements at both the temperatures was higher when compared to *U* displacements, and this is due to the presence of significant number of *V* fringes at the reference state, as discussed earlier. However, the error is still within the acceptable range for model validation.

CHAPTER VIII

AUTOMOTIVE FIELD-USE CORRELATION WITH ACCELERATED THERMAL CYCLING

The number of accelerated thermal cycles, the temperature range and the time of dwell used for qualifying a microelectronic package should be based on the type of application the package is intended for. However, the industry practice is legacy based and not physics-based. Therefore, the present work focuses on using a physics-based mapping methodology for estimating the number of cycles required to qualify a package when used under automotive field-use conditions. A common feature of the physics-based failure prediction models is that a damage metric or a failure indicator is used for estimating the number of cycles to fatigue failure. Accumulated inelastic stain, strain range and accumulated inelastic strain energy density are the three damage metrics that were used for the present work. The SBGA 352 package was used as a representative package to determine the field-use correlation. Both linear and non-linear mapping of these damage metrics were used to estimate the number of cycles that will be required to qualify a package.

As was explained in section 2.10, the solder material undergoes both time dependent creep deformation and time-independent plastic deformation. Creep deformation is due to diffusion flow of vacancies whereas plastic flow is due to movement of dislocations. The percentage contribution of these two deformation mechanisms to the total deformation is different for field-use

conditions and for standard accelerated thermal cycling. Hence, alternate thermal cycling guidelines based on non-linear and linear strain mapping were developed and will be presented in this work.

8.1 Automotive Field-Use Conditions

Electronic systems used in automobiles experience different field-use temperature regimes during different seasons. Table 8.1 shows the summary of the field–use conditions experienced by an automobile. The maximum and the minimum temperatures and the ramp rates were obtained for the under the hood application in the vehicle frontal zone [Hellemans and Lewandowski, 1993, Jurgen, 1995]. The dwell time at high temperature is based on the average driving time to work and back, and for other daily chores. It is assumed that an automobile is driven to work, parked for about nine hours and driven back from work and parked for the rest of the day. The average driving time per day is assumed to be two and a half hours. It is also assumed that such a driving is performed 300 days a year with 100 days each in summer, winter and spring seasons for 10 years [Syed and Doty, 1999]. The temperature ramp down rate upon parking was assumed to be half that of temperature ramp up rate during driving from the parked state.

Table 8.1 Automotive field-use conditions

SBGA 352 for Automotive Application Vehicle Frontal Zone	Tmax (°C)	Tmin (°C)	Driving time (hh:mm)	Idle time(hh:mm)	No. of days during 10 years
Summer	85	25	2:30	21:30	1000
Spring	85	0	2:30	21:30	1000
Winter	85	-40	2:30	21:30	1000

Figures 8.1 through 8.3 show the thermal cycling profiles that the package experiences on a particular day during three different seasons.

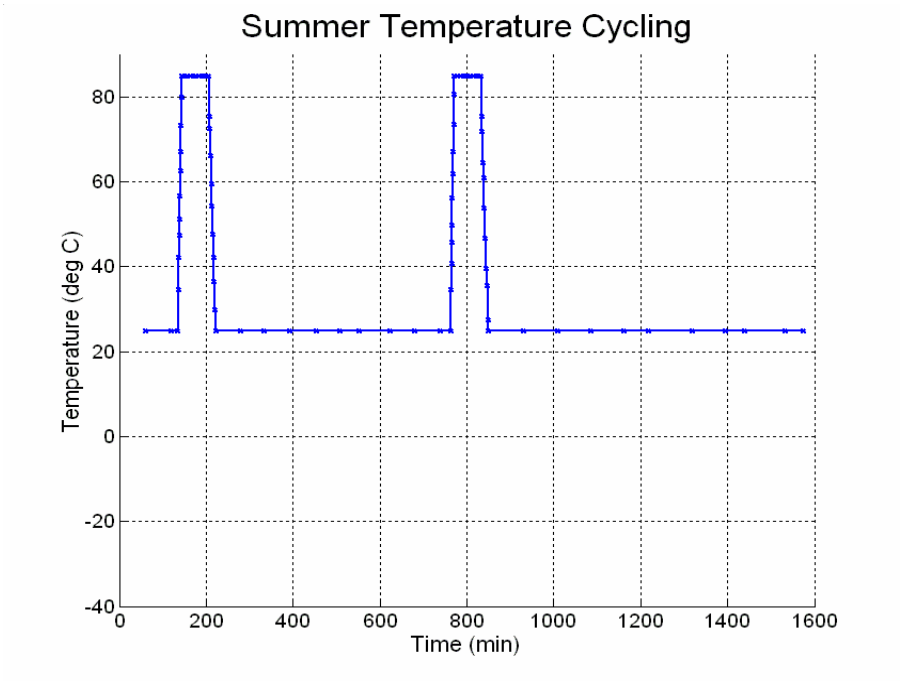


Figure 8.1 Temperature profile experienced during a typical summer day

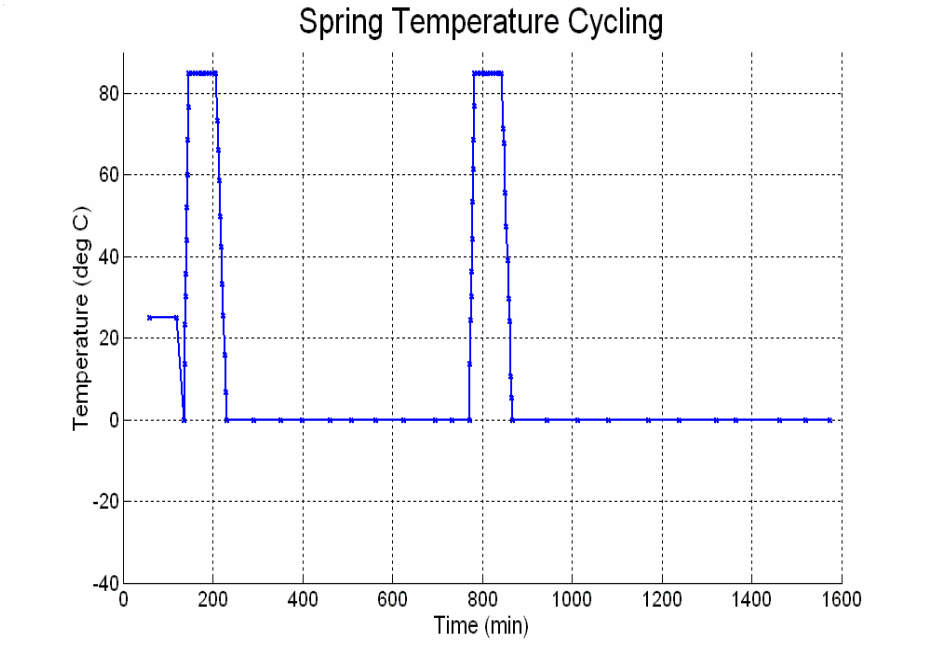


Figure 8.2 Temperature profile experienced during a typical spring day

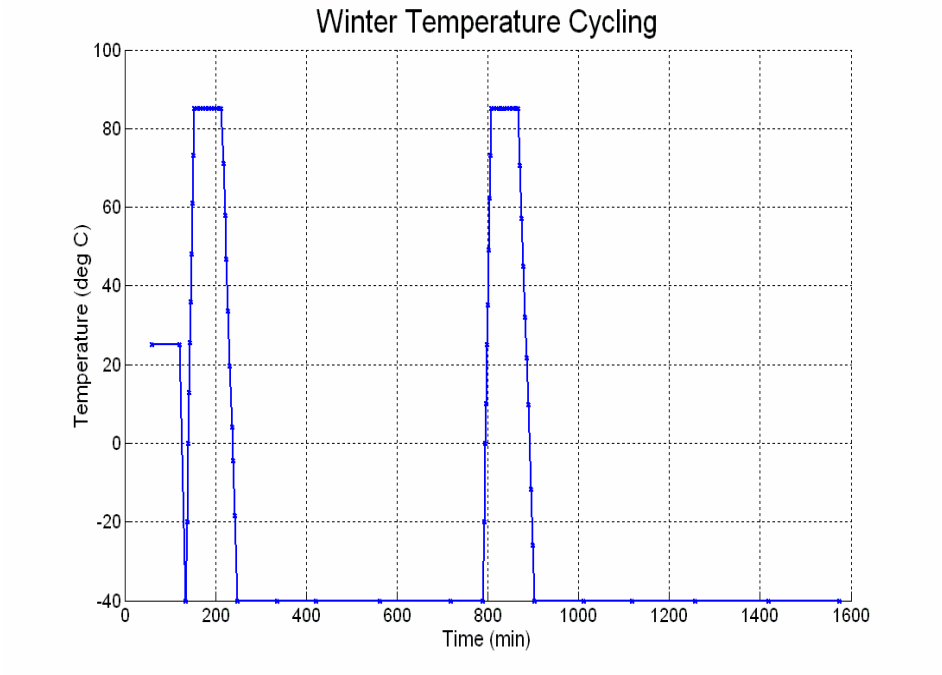


Figure 8.3 Temperature profile experienced during a typical winter day

Numerical simulations were performed on the SBGA package using the GPD model geometry which was explained in section 4.3.2. The elastic-plastic-creep model, as given in section 6.2.1, was used for modeling the solder joint material behavior. The accumulated inelastic strains, accumulated inelastic strain energy density and the inelastic strain range experienced by the package during one day was determined. The results for the analysis are shown in Table 8.2.

Table 8.2 Damage metric values per day during field-use conditions

SBGA 352	Acc. Inelastic Strain	Acc. Inelastic Energy density (N/mm^2)
Spring	0.003857031	0.040147012
Summer	0.002344307	0.020218425
Winter	0.004928409	0.067577153

The damage metric values given in Table 8.2 can also be broken down into their creep and plastic parts. Table 8.3 through Table 8.5 shows the decomposed damage metric values.

Table 8.3 Decomposed values of accumulated strains

Accumulated strains	Acc. Plastic Strain	Acc. Creep Strain	Acc. Inelastic Strain
Spring	0.00244880	0.00142202	0.00385703
Summer	0.00098553	0.00136506	0.00234431
Winter	0.00421046	0.00073287	0.00492841

Table 8.4 Decomposed values of accumulated strain energy density

Accumulated strain energy density	Acc. plastic strain energy density (N/mm^2)	Acc. creep strain energy density (N/mm^2)	Acc. inelastic strain energy density (N/mm^2)
Spring	0.02609251	0.01417793	0.04014701
Summer	0.00863021	0.01163948	0.02021842
Winter	0.06032410	0.00741022	0.06757715

Table 8.5 Decomposed values of strain range

Strain range	Acc. Plastic Strain range	Acc. Creep Strain range	Acc. inelastic strain range
Spring	0.00067957	0.00080692	0.00131188
Summer	0.00030616	0.00078681	0.00097036
Winter	0.00113682	0.00046811	0.00139330

8.2 Linear Damage Mapping

Linear damage mapping that was dealt with in section 2.9.1 can now be used to estimate the number of cycles required to quality a package. Linear damage mapping is based on the assumption that the number of cycles to failure is inversely proportional to the inelastic strain energy density or to the inelastic strain accumulated in one thermal cycle. Linear mapping linearly sums the damage metric over the entire field-use. By dividing this summed damage metric by the damage metric in one ATC, the number of ATC required to qualify

a package is determined. The field-use conditions can often be broken down into similar operating conditions based on seasons, temperature range experienced etc. If p_i represents the number of cycles that the package experiences under each such operating conditions, then the number of cycles required to qualify a package by strain and energy based criterion is given by equations 8.1 and 8.2 respectively.

$$N_E{}^l = \frac{\sum_i p_i (\Delta W_{ave,acc})_i}{(\Delta W_{ave,acc})_{ATC}} \qquad \text{Eq (8.1)}$$

$$N_S{}^l = \frac{\sum_i p_i (\Delta \varepsilon^{in}{}_{ave,acc})_i}{(\Delta \varepsilon^{in}{}_{ave,acc})_{ATC}} \qquad \text{Eq (8.2)}$$

Table 8.6 shows the strains and energy densities accumulated at a critical solder joint in one MIL-STD-883E-condition B accelerated thermal cycle.

Table 8.6 Damage metric values during ATC for linear mapping

Damage metric	Value
Accumulated inelastic strain	0.004802800
Accumulated inelastic strain energy density	0.062923127 N/mm^2

Using the results from Table 8.2 and 8.6 in equation 8.1 and 8.2 and using 1000 days of usage per season as the design life of the package for 10 years, the number of cycles required to qualify the package and the time required to qualify it can be obtained. This is shown in Table 8.7.

Table 8.7 Qualification cycles and times for linear damage mapping

	Number of cycles	Qualification Time (hh:mm)
Strain based	2317	2317:00
Energy based	2033	2033:00

8.3 Non-Linear Damage Mapping

The equations governing non-linear damage mapping has been explained in section 2.9.2. Non-linear mapping requires us to decompose the accumulated inelastic strain energy density and inelastic strain range into their creep and plastic components. Table 8.8 shows the results from the simulations when the package is subjected to MIL-STD-883E-condition B thermal cycling condition.

Table 8.8 Damage metric values during ATC for non-linear mapping

	Plastic	Creep
Strain range	0.002148	0.000817
Accumulated strain energy density	0.056419 N/mm^2	0.006774 N/mm^2

The results from table 8.8 can now be combined with the results from the Table 8.3, 8.4 and 8.5 using equations 2.29 and 2.31 to obtain the number of cycles required to qualify the package using non-linear mapping methodology. Table 8.9 shows the results from the analysis.

Table 8.9 Qualification cycles and times for non-linear mapping

	Number of cycles	Qualification Time (hh:mm)
Strain based	1876	1876:00
Energy based	1734	1734:00

8.4 Alternate Thermal Cycling

Field-use is characterized by long dwell times during operational and diurnal use (parked automobile). During these dwell times the solder continues to creep and the percentage of creep deformation increases. As a consequence, during field-use, solder undergoes more creep deformation compared to what is captured in accelerated thermal cycling. Tables 8.10 and 8.11 show the creep deformation during each day of field-use in of the three seasons.

Table 8.10 Calculation of percentage of accumulated creep energy during field-use

Season	Total acc pl energy density (N/mm^2)	Total acc creep energy density (N/mm^2)	Total acc inelastic energy density (N/mm^2)	% Creep
Spring	0.02609251	0.01417793	0.04014701	35.31503629
Summer	0.00863021	0.01163948	0.02021842	57.56866848
Winter	0.06032410	0.00741022	0.06757715	10.96557334
			AVERAGE CREEP:	**25.97073588**

Table 8.11 Calculation of percentage of accumulated creep strain during field-use

Season	Total acc pl strain	Total acc creep strain	Total acc inelastic strain	% Creep
Spring	0.00244880	0.00142202	0.00244880	36.868288320
Summer	0.00098553	0.00136506	0.00098553	58.228539081
Winter	0.00421046	0.00073287	0.00421046	14.870298183
			AVERAGE CREEP:	**31.626470669**

It can be seen from Table 8.10 and Table 8.11 that the percentage creep from energy based criteria is around 26% and from the strain based criteria it is around 32%. Table 8.12 shows the percentage creep as observed during MIL-STD-883E-condition B thermal cycling.

Table 8.12 Calculation of percentage creep during baseline ATC

ATC	Plastic	Creep	Inelastic	% Creep
Accumulated strain	0.003941734	0.000892489	0.004802800	**18.5827**
Accumulated strain energy density (N/mm^2)	0.056419888	0.006774465	0.062923127	**10.7662**

Comparing the field-use results from Table 8.10 and 8.11 with the ATC results from Table 8.12, we can see that the ATC does not capture the creep deformation of the solder adequately. The MIL-STD-883E baseline ATC should hence be altered to change this percent contribution.

There are many ways to increase the percent creep contribution. Creep strain depends on temperature and stress relaxation. Higher the temperature and higher the time allotted for stress relaxation, higher is the creep strain contribution. This would mean that the low dwell and high dwell temperatures should be increased and/or the dwell times at these temperatures should be increased. In the present work, it was found that increasing the dwell time at both high and low temperatures increased the creep contribution only marginally. Hence, only the effect of increasing high and low dwell temperatures was investigated. Changing the temperature ramp rate can also affect the percent creep contribution. However, in the present work, the effect of changing the ramp rates was not investigated.

8.4.1 Alternate Thermal Cycling 1

As a first step towards increasing the percent creep contribution, the lower dwell temperature was increased from -55°C to 0°C. Since a long dwell at the lower temperature does not add to the creep deformation significantly, the

lower dwell time duration was decreased. This decrease would provide us the added bonus of being able to qualify a package quickly using an ATC with lesser cycle time. However, the low dwell temperature cannot be lowered arbitrarily. Figure 8.4 shows a plot of temperature setting inside a thermal chamber and the actual temperature experienced by the package. It can be seen that it takes about 4.5 minutes for the package to reach within 10 degrees of the high dwell temperature and about 5 minutes for the package to reach within 10 degrees of the low dwell temperature. Keeping this in mind, the time for low dwell was reduced from 20 minutes to 6 minutes. The cycle time for this ATC was 39 minutes 53 seconds.

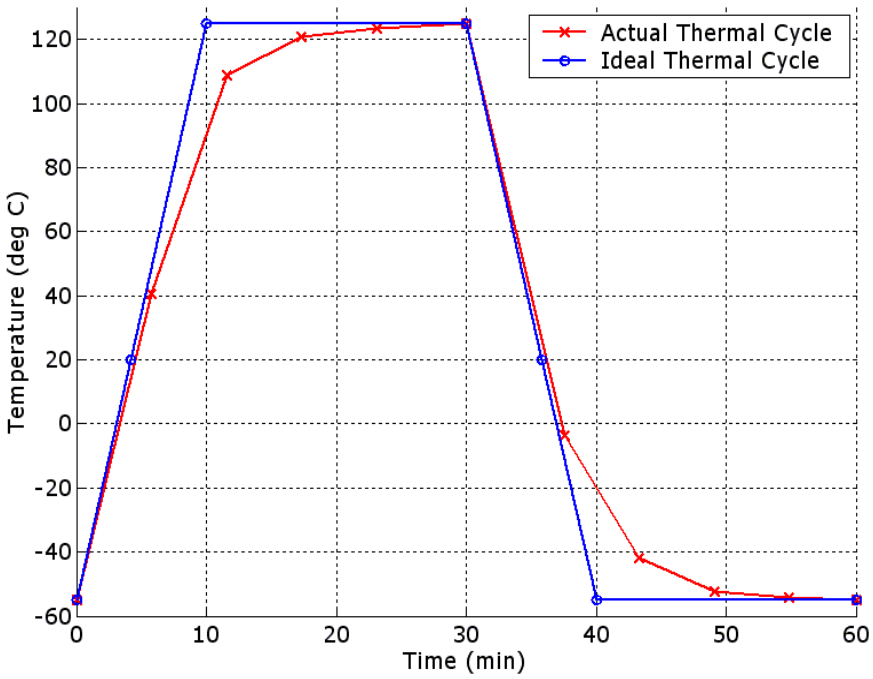


Figure 8.4 Thermal profile experienced by the package cycled in a thermal chamber

Table 8.13 shows the calculation of percentage creep obtained by using numerical analysis.

Table 8.13 Calculation of percentage creep during alternate ATC 1

Alltenate 1	Plastic	Creep	Inelastic	% Creep
Accumulated strain	0.002194502	0.0006680377	0.002848426	**23.4529**
Accumulated strain energy density (N/mm^2)	0.022624433	0.004957717	0.027471836	**18.0465**

We can see that the percent creep has still not matched the field use percentage given in Table 8.12. So, further modification of the thermal cycling regime is necessary.

8.4.2 Alternate Thermal Cycling 2

We noticed from the section 8.4.1 that increasing the lower dwell temperature from -55°C to 0°C did not help to increase the percent creep present in the solder joint to the extent we want it to be. As a next step, both the low and high dwell temperatures were increased. The low dwell temperature was increased from 0°C to 25°C and the high dwell temperature was increased from 125°C to 150°C. The dwell times were however kept constant. The cycle time for this ATC was 39 minutes 53 seconds. Table 8.14 show the results got from numerical analysis.

Table 8.14 Calculation of percentage creep during alternate ATC 2

Alternate 2	Plastic	Creep	Inelastic	% Creep
Accumulated strain	0.002702956	0.0010792994	0.003767773	**28.6456**
Accumulated strain energy density (N/mm^2)	0.021917741	0.008078986	0.02988154	**27.0367**

The percent creep found by this method is acceptable and can be used to qualify the solder joints for its reliability. However, the qualification time could be reduced further. Section 8.4.3 illustrates this method.

8.4.3 Alternate Thermal Cycling 3

The thermal cycling scheme developed above can be used to qualify a package satisfactorily. This section deals with the modification of the alternate thermal cycling 2 to decrease the time needed to qualify a package. The dwell time at high temperature was lowered from 20 minutes to 6 minutes. This would reduce the percent creep. So to compensate for this reduction, the low dwell temperature was increased to 45°C. The cycle time for this thermal cycle was 23 minutes 40 seconds. Table 8.15 shows the results for this simulation.

Table 8.15 Calculation of percentage creep during alternate ATC 3

Alternate 3	Plastic	Creep	Inelastic	% Creep
Accumulated strain	0.002124905	0.0008990823	0.003013215	**29.8380**
Accumulated strain energy density (N/mm^2)	0.015178158	0.006407337	0.021510753	**29.7866**

The percent creep is now closer to that of field-use and is acceptable.

8.5 Qualifying for Brittle Failures at Low Temperatures

It should be noted that while developing alternate thermal cycling guidelines to match the percentage of creep strain and creep energy, it might be necessary to increase the low dwell temperature significantly higher than the lowest temperature during field-use condition, which in the present case is -40°C. Doing this might not capture the failures modes during ATC which could have

the possibility of occurring during field-use. At temperatures as low as -40°C , the failures modes in the solder joint and in the package as a whole, are mainly due to brittle processes which occur instantaneously as against to ductile processes which occur gradually. Hence, if the alternate thermal cycle is designed such that the low dwell temperature is significantly higher than the lowest temperature observed during field-use, it would be necessary to include few accelerated thermal cycles which would capture the brittle failure behavior at low temperatures.

The alternate thermal cycle developed in section 8.4.3 had a minimum temperature of 45°C. The lowest dwell temperature in the present case is much higher that the lowest temperature observed during field-use. A thermal cycle with lowest temperature of -40°C and highest temperature of 85°C, with 6 minutes dwell at these two temperatures and with the same ramp rate as that of MIL-STD-883E was hence chosen to qualify the package at low temperature. The cycle time for one such thermal cycle will be 25 minutes 53 seconds. Table 8.16 shows the results from simulation performed at this condition.

Table 8.16 Simulation results for the thermal cycling between -40°C to 85°C with 6 minute dwell

Parameter	Value
Accumulated plastic strain	0.00208896
Accumulated creep strain	0.00032592
Accumulated inelastic strain	0.00240391
Accumulated plastic energy density	0.02840007 (N/mm^2)
Accumulated creep energy density	0.00290825 (N/mm^2)
Accumulated inelastic energy density	0.03120369 (N/mm^2)
Plastic strain range	0.00109587
Creep strain range	0.00031816
Inelastic strain range	0.00122257
Cycle time	25 min 53 min

Assuming 100 such thermal cycles, it would take 43 hours and 8 minutes to qualify the package at low temperatures.

The results obtained from alternate thermal cycle 3 can now be used along with field use conditions given in Table 8.2 through 8.6 to obtain the number of cycles required to qualify a package and the cycle time that is needed for qualification. The damage that occurs by the 100 cycles mentioned above should be factored into before making an estimate on the number of cycles. Linear and non-linear strain based damage mapping, as given in section 2.9, were used to determine the number of cycles and the qualification time. Table 8.17 summarizes the result.

Table 8.17 Summary of results for alternate thermal cycling 3

Alternate 3	Number of cycles	Qualification time (hh)
Linear strain based	3613	1425
Non-linear strain based	2792	1144

8.6 Summary of damage mapping and qualification times

From Table 8.7 and 8.9 we can see that the maximum number of cycles required to map the damage occurring in the solder is 2317 cycles. The experimental thermal cycling of SBGA packages conducted at Georgia Tech showed that the packages survived for more than 3000 cycles. Hence, we can consider the package to be qualified for automotive field-use condition.

Table 8.18 shows the summary of the time needed to qualify an SBGA 352 package under automotive field use conditions for both MIL-STD-883E thermal cycling conditions and alternate thermal cycling conditions.

Table 8.18 Summary of linear and non-linear mapping methods based on strain and energy based mapping

Method	Baseline MIL-STD-883E (hh)	Alternate 3 ATC (hh)
Linear strain based	2317	1425
Linear energy based	2033	-
Non-linear strain based	1876	1144
Non-linear energy based	1734	-

From Table 8.18 we can see that linear mapping methods estimate a higher number of cycles required to qualify a package. Hence, they are conservative. Alternate ATC 3 takes care to match the percent of creep during accelerated thermal cycling to the percent of creep during field-use condition. By doing so, the qualification time can be reduced by almost 700 hours.

CHAPTER IX

CONCLUSIONS AND FUTURE WORK

9.1 Conclusions

Two different packages, PBGA and SBGA, were studied for thermo-mechanical reliability assessment of solder joints using 62Sn36Pb2Ag solder. For the PBGA package, the effect of six different combinations of mold and die-attach compounds on the solder joint reliability was assessed using a preliminary 2D model. The worst case combination was chosen for further reliability studies using GPD and 3D models. Moiré interferometry was used as a means to validate the modeling methodology by comparing the in-plane displacements occurring in the cut sample with the displacements obtained by FEA. Excellent agreement was obtained between the results obtained by finite element analysis and experiments. It was found that the average percent error of the displacements obtained from modeling decreases as we go away from the reference temperature at which the grating was applied. The percentage error in the *U* displacement was found to be lower than the percentage error in the *V* displacement at all the temperatures. Fatigue life for mean failure and 1% failure was estimated. The fatigue life estimated by the GPD model matches closely with the fatigue life estimated by the 3D model. However, the failure location predicted by both the models was found to be different.

For the SBGA package, a GPD model was used to assess the reliability of the solder joints. The SBGA packages were assembled on a test vehicle and subjected to accelerated thermal cycling with MIL-STD-883 E thermal cycling regime. The resistance of the solder joints was monitored and a 100% increase in resistance of the daisy chain was used to determine failure of the package. The change in the resistance of the solder ball as a function of thermal cycling was determined using electro-static FEA analysis. The 100% change in daisy chain resistance was obtained from FEA and excellent match was found between the results obtained from FEA and thermal cycling. Moire interferometry was used to find the in-plane displacements in the *U* and *V* directions. Excellent correlation was found between the experimental results and the results obtained from FEA analysis.

Linear and non-linear damage mapping was performed on the SBGA package using accumulated inelastic strain and accumulated inelastic strain energy density as damage metrics. For the automotive field-use conditions, the linear mapping methodology predicted that we need to subject the package for 2300 MIL-STD thermal cycles. Non-linear mapping using the fatigue life equation of the 62Sn36Pb2Ag solder, however, gives a better estimate of around 1800 cycles to qualify the package. The mapping cycles determined by strain method was always found to be higher when compared to the mapping cycles obtained by the energy method.

The MIL-STD thermal cycle was found not to replicate the actual deformation mechanism occurring in the solder during its field-use operation. For the automotive field-use application, the solder joints were found to accumulate

about 32% of deformation due to creep. However, during the MIL-STD ATC, the solder joint was found to accumulate only 18% of the deformation due to creep. The same trend was found for the accumulation of creep energy density too. The possible reason for such high accumulation of creep during field-use is due to the presence of long hours of dwell time while the vehicle is being driven and while the vehicle is being parked.

Alternate thermal cycles were designed to match the percentage of accumulated creep strain and accumulated creep energy density occurring during field-use and thermal cycling. The percentage contribution of creep strain was increased by varying the dwell time and dwell temperatures. The alternate thermal cycling that were redesigned had a low dwell temperature of 45°C and a high dwell temperature of 150°C. It was found that increasing the dwell time at both high and low temperatures increased the creep contribution only marginally. Hence, the dwell times at these two temperatures were reduced to reduce the cycle time for accelerated thermal cycling. The redesigned alternate thermal cycling had a cycle time of 23 minutes and 40 seconds and by adopting this cycle, the total qualification time can be reduced by almost 700 hours.

9.2 Contributions

- The reliability of SBGA and PBGA assemblies on an organic substrate was studied by developing numerical models using temperature, time and direction dependent properties.

- Finite element parametric models developed were validated using thermal cycling experimental data and moiré interferometry.
- The effect of different combinations of mold and die-attach compounds on the solder joint fatigue was determined for the PBGA package.
- Linear and non-linear mapping methodologies were introduced and were used to estimate the number of standard cycles needed to qualify an SBGA package subjected to automotive field conditions.
- The effects of using two different damage metrics, strain-based and energy-based, to determine the required number of cycles needed for qualification were investigated.
- A methodology of varying the contributions of creep and plastic strain to total inelastic strain was developed to match the contributions of grain sliding and dislocation movement to total accumulated strain occurring in the solder.

9.3 Future Work

The material property of the solder joint was assumed to be constant during thermal cycling. In reality, the modulus of the solder material decreases during fatigue due to the presence of micro-voids which gradually increase in size. Damage mechanics approach that includes the change in the constitutive behavior of the solder would be more representative of the actual behavior of the solder material during fatigue.

The field-use mapping methodology described in the paper does not describe the evolution of the grain structure. The number of qualification cycles obtained by mapping the evolution of the grain structure during field-use and ATC would be more indicative of the damage occurring in the solder.

The techniques outlined in this work can be extended to lead-free solder joints as well.

APPENDIX A

SURFACE EVOLVER CODE TO FIND THE SOLDER JOINT GEOMETRY

A1. SOLDER BALL GEOMETRY IN A SBGA PACKAGE

```
// Simple ball grid array joint.
// Circular, parallel, coaxial wetted pads in fixed positions.
// The liquid is entirely bounded by facets.

// Shape parameters
parameter S_TENSION = 480 //liquid solder surface tension, erg/cm^2
parameter SOLDER_DENSITY = 9 // grams/cm^3
gravity_constant 980     // cm/sec^2

//THE SOLDER BALL IS SOLDER MASK DEFINED ON BOTH THE SIDES
parameter height = 0.686*1e-1 //STANDOFF HEIGHT IN cm
parameter radiust = (0.25)*1e-1    // radius of top pad, cm
parameter radiusb = (0.254)*1e-1       //radius of the bottom pad,cm
parameter vol_sol = 0.31e-3 //volume in cm3 OBTAINED BY PERSONAL COMMUNICATIONS

// rim of pads (need something to keep pads circular when refined)
constraint 1
formula: x^2 + y^2 = radiust^2

constraint 2
formula: x^2 + y^2 = radiusb^2
```

constraint 3

formula: z = 0

constraint 4

formula: z = height

vertices

// lower pad

1 radiusb*cos(0*pi/3) radiusb*sin(0*pi/3) 0 constraints 2,3 fixed

2 radiusb*cos(1*pi/3) radiusb*sin(1*pi/3) 0 constraints 2,3 fixed

3 radiusb*cos(2*pi/3) radiusb*sin(2*pi/3) 0 constraints 2,3 fixed

4 radiusb*cos(3*pi/3) radiusb*sin(3*pi/3) 0 constraints 2,3 fixed

5 radiusb*cos(4*pi/3) radiusb*sin(4*pi/3) 0 constraints 2,3 fixed

6 radiusb*cos(5*pi/3) radiusb*sin(5*pi/3) 0 constraints 2,3 fixed

// upper pad

7 radiust*cos(0*pi/3) radiust*sin(0*pi/3) height constraints 1,4 fixed

8 radiust*cos(1*pi/3) radiust*sin(1*pi/3) height constraints 1,4 fixed

9 radiust*cos(2*pi/3) radiust*sin(2*pi/3) height constraints 1,4 fixed

10 radiust*cos(3*pi/3) radiust*sin(3*pi/3) height constraints 1,4 fixed

11 radiust*cos(4*pi/3) radiust*sin(4*pi/3) height constraints 1,4 fixed

12 radiust*cos(5*pi/3) radiust*sin(5*pi/3) height constraints 1,4 fixed

edges // defined by endpoints

// lower pad edges

1 1 2 constraints 2,3 fixed

2 2 3 constraints 2,3 fixed

3 3 4 constraints 2,3 fixed

4 4 5 constraints 2,3 fixed

5 5 6 constraints 2,3 fixed

6 6 1 constraints 2,3 fixed

// upper pad edges

7 7 8 constraints 1,4 fixed

8 8 9 constraints 1,4 fixed

9 9 10 constraints 1,4 fixed

10 10 11 constraints 1,4 fixed

11 11 12 constraints 1,4 fixed

12 12 7 constraints 1,4 fixed

// vertical edges between top and bottom copper pad

13 1 7

14 2 8

15 3 9

16 4 10

17 5 11

18 6 12

faces // defined by oriented edge loops to have outward normal

// lateral faces between top and bottom copper pad

1 1 14 -7 -13 tension S_TENSION

2 2 15 -8 -14 tension S_TENSION

3 3 16 -9 -15 tension S_TENSION

4 4 17 -10 -16 tension S_TENSION

5 5 18 -11 -17 tension S_TENSION

```
6   6 13 -12 -18 tension S_TENSION

// lower pad

7   1 2 3 4 5 6 fixed no_refine color red tension 0 constraint 3

// upper pad

8    7  8  9 10 11 12 fixed no_refine color green tension 0 constraint 4


bodies // defined by oriented face list

1   1 2 3 4 5 6 7 8 volume vol_sol density SOLDER_DENSITY //volume in cm3


read

hessian_normal // to make "hessian" work better


// Typical evolution

//EVOLVE IS A FILE THAT OUTPUTS 3 FILES CONTAINING THE INFORMATION ABOUT VERTICES,

EDGES AND FACETS

read "evolve.txt"
```

A2. SOLDER BALL GEOMETRY IN A PBGA PACKAGE

```
// Simple ball grid array joint.

// Circular, parallel, coaxial wetted pads in fixed positions.

// The liquid is entirely bounded by facets.


// Shape parameters

parameter S_TENSION = 480 //liquid solder surface tension,  erg/cm^2

parameter SOLDER_DENSITY = 9 // grams/cm^3

gravity_constant 980     // cm/sec^2
```

//THE SOLDER BALL IS SOLDER MASK DEFINED ON THE PACKAGE SIDE AND COPPER PAD DEFINED ON THE BOARD SIDE

// height of upper pad, cm

parameter height = 0.508*1e-1//AVERAGE STANDOFF HEIGHT IN cm

parameter radiust = (0.61138/2)*1e-1 // radius of top pad, cm

parameter radiusb = (0.5842/2)*1e-1 //radius of the bottom pad,cm

parameter vol_sol = 0.23399e-3 //volume in cm3 got by personal communications

parameter thickbot = 0.04064*1e-1 //thickness of the bottom copper pad

// rim of pads (need something to keep pads circular when refined)

constraint 1

formula: x^2 + y^2 = radiust^2

constraint 2

formula: x^2 + y^2 = radiusb^2

constraint 3

formula: z = 0

constraint 4

formula: z = height

constraint 5

formula: z = thickbot

vertices

```
// lower pad
1  radiusb*cos(0*pi/3) radiusb*sin(0*pi/3) 0 constraints 2,3 fixed
2  radiusb*cos(1*pi/3) radiusb*sin(1*pi/3) 0 constraints 2,3 fixed
3  radiusb*cos(2*pi/3) radiusb*sin(2*pi/3) 0 constraints 2,3 fixed
4  radiusb*cos(3*pi/3) radiusb*sin(3*pi/3) 0 constraints 2,3 fixed
5  radiusb*cos(4*pi/3) radiusb*sin(4*pi/3) 0 constraints 2,3 fixed
6  radiusb*cos(5*pi/3) radiusb*sin(5*pi/3) 0 constraints 2,3 fixed
// upper pad
7  radiust*cos(0*pi/3) radiust*sin(0*pi/3) height constraints 1,4 fixed
8  radiust*cos(1*pi/3) radiust*sin(1*pi/3) height constraints 1,4 fixed
9  radiust*cos(2*pi/3) radiust*sin(2*pi/3) height constraints 1,4 fixed
10 radiust*cos(3*pi/3) radiust*sin(3*pi/3) height constraints 1,4 fixed
11 radiust*cos(4*pi/3) radiust*sin(4*pi/3) height constraints 1,4 fixed
12 radiust*cos(5*pi/3) radiust*sin(5*pi/3) height constraints 1,4 fixed
// top of bottom copper pad
13  radiusb*cos(0*pi/3) radiusb*sin(0*pi/3) thickbot constraints 2,5    fixed
14  radiusb*cos(1*pi/3) radiusb*sin(1*pi/3) thickbot constraints 2,5    fixed
15  radiusb*cos(2*pi/3) radiusb*sin(2*pi/3) thickbot constraints 2,5    fixed
16  radiusb*cos(3*pi/3) radiusb*sin(3*pi/3) thickbot constraints 2,5    fixed
17  radiusb*cos(4*pi/3) radiusb*sin(4*pi/3) thickbot constraints 2,5    fixed
18  radiusb*cos(5*pi/3) radiusb*sin(5*pi/3) thickbot constraints 2,5 f  ixed


edges  // defined by endpoints
// lower pad edges
1    1  2  constraints 2,3 fixed
2    2  3  constraints 2,3 fixed
```

3 3 4 constraints 2,3 fixed

4 4 5 constraints 2,3 fixed

5 5 6 constraints 2,3 fixed

6 6 1 constraints 2,3 fixed

// upper pad edges

7 7 8 constraints 1,4 fixed

8 8 9 constraints 1,4 fixed

9 9 10 constraints 1,4 fixed

10 10 11 constraints 1,4 fixed

11 11 12 constraints 1,4 fixed

12 12 7 constraints 1,4 fixed

// vertical edges between top and bottom copper pad

13 1 7

14 2 8

15 3 9

16 4 10

17 5 11

18 6 12

// edges top of bottom copper pad

19 13 14 constraints 2,5 fixed

20 14 15 constraints 2,5 fixed

21 15 16 constraints 2,5 fixed

22 16 17 constraints 2,5 fixed

23 17 18 constraints 2,5 fixed

24 18 13 constraints 2,5 fixed

```
// vertical edges between top and top of bottom copper pad
25 1 13 constraints 2 fixed
26 2 14 constraints 2 fixed
27 3 15 constraints 2 fixed
28 4 16 constraints 2 fixed
29 5 17 constraints 2 fixed
30 6 18 constraints 2 fixed

faces // defined by oriented edge loops to have outward normal
// lateral faces between top and bottom copper pad
1   1 14  -7 -13 tension S_TENSION
2   2 15  -8 -14 tension S_TENSION
3   3 16  -9 -15 tension S_TENSION
4   4 17 -10 -16 tension S_TENSION
5   5 18 -11 -17 tension S_TENSION
6   6 13 -12 -18 tension S_TENSION
// lower pad
7   -24 -23 -22 -21 -20 -19 fixed no_refine color red tension 0 constraint 5
// upper pad
8    7  8  9 10 11 12 fixed no_refine color green tension 0 constraint 4

//lateral faces between bottom and top of bottom copper pad
9 -1 25 19 -26 color blue constraints 2 fixed
10 -2 26 20 -27 color blue constraints 2 fixed
11 -3 27 21 -28 color blue constraints 2 fixed
12 -4 28 22 -29 color blue constraints 2 fixed
```

```
13 -5 29 23 -30 color blue constraints 2 fixed

14 -6 30 24 -25 color blue constraints 2 fixed


bodies // defined by oriented face list

1   1 2 3 4 5 6 7 8 9 10 11 12 13 14 volume vol_sol density SOLDER_DENSITY //volume in cm3

read // commands to be automatically executed after loading the surface

hessian_normal // to make "hessian" work better


// Typical evolution

read "evolve.txt"
```

A3. Evolver Routine

```
s //used to get the GUI window

q //graphic  command

g 500 //perform the energy minimization algorithm 500 times

r//perform refinement of the mesh

g 500

r

g 150

r

g 50

list vertices >>> "vlist.txt"          //output a file containing list of vertices

list edges >>> "elist.txt" //output a file containing list of elements

list facets >>> "flist.txt"  //output a file containing list of facets
```

REFERENCES

Abtew. M., and Selvaduray. Guna., "Lead-Free Solders in Microelectronics", *Material Science and Engineering*, Vol 27, pp. 95-141, 2000

Amkor 2000, Material properties data sheet and mechanical drawings, received via company email. Unpublished proprietary data. Westchester, PA.

Anand, L. 1985, "Constitutive Equations for Hot-Working of Metals", *International Journal of Plasticity*, vol. 1, no. 3, pp. 213-231

Ansys, Inc. Theory Manual., Release 5.7. ch. 14, pp. 107, 1994

Bae Systems, 2003, Manufacturing data sheets and through personal communications

Barker, D.B., Dasgupta, A. 1993, "Thermal Stress Issues in Plated-Through-Hole Reliability," *Thermal Stress and Strain in Microelectronics Packaging*, J. H. Lau (ed.), Van Nostrand Reinhold, New York

Brakke, K. A., *The Motion of a Surface by its Mean Curvature,* Princeton University Press, Princeton, NJ, 1977.

Brakke, K. A., "The Surface Evolver", *Experimental Mathematics,* Vol. 1, No. 2, pp, 142-165, 1992.

Busso, E. P., and Kitano, M., 1992, "A Visco-Plastic Constitutive Model for 60/40 Tin-Lead Solder Used in IC Package Joints," *ASME J. Eng. Mater Technology.,* 114. pp, 331-337.

ChipPAC Incorporated, 2000, *PBGA Product Guide*, [ChipPAC Incorporated Product Guide], [Online]. Available: http://www.chippac.com/download/ChipPACPBGAProductGuide(Rev2000.11.07).pdf. ChipPAC, Inc. Copyright © 2000.

Dai, F., McKelvie, J and Post, D., "An Interpretation of Moire Interferometry from Wavefront Interference Theory", *Optics and Lasers in Engineering,* Vol. 12, pp. 101-118, 1990.

Darveaux, R., Banerji, K. 1992, "Constitutive Relations for Tin-Based Solder Joints," *Proc. 50th Electronic Components and Technology Conference*, IEEE, San Diego, CA, pp. 538-551.

Darveaux, R. 1997, "Solder Joint Fatigue Life Model", *Proc. Symp. Design and Reliability of Solders and Solder Interconnections, TMS Annual Meeting*, Minerals, Metals & Materials Soc, Orlando, FL, USA, 10-13

Darveaux, R., "Effect of Simulation Methodology on Solder Joint Crack Growth Correlation", *50th IEEE-ECTC,* pp. 1048-1058, May 2000

Derman, G., "IC Attachments, Interconnects & Packaging," *Electronic Engineering Times,* February, 28th, 1994, pp. 44-51.

Engelmaier, W. 1983, "Fatigue Life of Leadless Chip Carrier Solder Joints During Power Cycling", *IEEE Trans. on Components, Packaging, and Manufacturing Technology,* IEEE, vol. CHMT-6, No. 3, pp. 52-57.

Freyman, B., and Pennisi, R., " Overmolded Plastic Pad Array Carriers (OMPAC): A Low Cost, High Interconnect Density IC Packaging Solution for Consumer and Industrial Electronics," *Proceedings of the 41th IEEE Electronic Components & Technology Conference,* Las Vegas, May 1991, pp. 176-182

Garofalo, F. 1965, *Fundamentals of Creep and Creep-Rupture in Metals*, The Macmillan Company, New York, NY.

Hall, P. M., and Sherry, W. M., 1986, " Materials. Structures and Mechanics of Solder Joints for Surface-mount Microelectronics Technology," *Proceedings of Conference of Interconnection Technology in Electronics.* Fellbach, W. Germany, Feb., pp. 47-61.

Han, B., and Guo, Y., "Thermal Deformation Analysis of Various Electronic Packging Products by Moire and Microscopic Moire Interferometry", *Journal of Electronic Packaging,* Vol. 117, pp.185-189, 1995.

Han, B., Post, D., and Ifju., P., *High Sensitivity Moire Experimental Analysis for Mechanics and Materials,* Springer-Verlag, pp. 332-333, 1994

Hellemans, R., and Lewandowski, P., "Low Cost Electronics Packaging for the Severe Automotive Environment"., *Electronic Packaging Forum – Multichip Module Technology Issues.,* Edited by Morris, J. E., IEEE Press, 1993

Iannuzzelli, R., "Predicting Plated-Through-Hole Reliability in High-Temperature Manufacturing Process," *Proc. of the 41st ECTC.,* 1991, pp.410-421

Interconnection Technology Research Institute 1998, *Ball Grid Array Packaging Guidelines*, Jet Propulsion Laboratory, California Inst. Tech.

Ju, S.H., Kuskowski, S., Sandor, B., and Plesha, M.E., 1994, "Creep- Fatigue Damage Analysis of Solder Joints", *Fatigue of Electronic Materials*, *ASTM STP 1153*, S.A. Schroeder and M.R. Mitchell, (eds), American Society for Testing and Materials, Philadelphia, PA, pp. 1-21.

Jurgen, R., "Automotive Electonics Handbook", McGraw Hill Publication, 1995

Knecht, S., Fox, L. 1991, "Integrated Matrix Creep: Application to Accelerated Testing and Lifetime Prediction," *Solder Joint Reliability --Theory and Applications*, J. Lau, (ed)., Van Nostrand Reinhold, New York, pp. 508-544.

Lau, J. H., "Ball Grid Array Technology". McGraw Hill Publications, 1995

Lau, J. H., and S. Erasmus, June 1993 "Review of Packaging Methods to Complement IC Performance," *Electronic Packaging & Production,* pp. 51-56.

Lau, J. H., and Pao, Y., "Solder Joint Reilabitity of BGA, CSP, Flip Chip, and Fine Pitch SMT Assemblies", McGraw Hill Publications, 1997

Lin, P., Lee, J., Im, S. 1970, "Design Considerations for a Flip-Chip Joining Technique." *Solid State Technology*, vol. 13, no. 7, pp. 48-54.

Lubliner, J., *Plasticity Theory,* Macmillan Publishing Company, 1990

Michaelides, S. 1999, *Physics-Based Process Modeling, Reliability Prediction, and Design Guidelines for Flip-Chip Devices*, PhD Thesis, School of Mechanical Engineering, Georgia Institute of Technology

McDowell, D.L., Miller, M.P. and Brooks, D.C. (1994). "A Unified Creep-Plasticity Theory for Solder Alloys", *Schroeder, S.A. and Mitchell, M.R. (eds.) Fatigue of Electronic Materials, ASTM STP 1153, American Society for Testing and Materials, Philadelphia*

Norris, K. C., Landzberg, A. H. 1969, "Reliability of Controlled Collapse Interconnects," *IBM Journal of Research and Development*, vol. 13, no. 3, pp. 266-271.

Oki Electric Industry Co., Ltd., 1997-2002, *OKI Silicon Solutions Company - Japan Site – Homepage* [Homepage of Oki Electric Industry Co., Ltd. Japan], [Online]. Available: http://www.oki.com/semi/english/package0.htm. Copyright © 1997-2002 Oki Electric Industry Company Ltd.

Pan, T., "Critical Accumulated Strain Energy (Case) Failure Criterion for Thermal Cycling Fatigue of Solder Joints", *Journal of Electronic Packaging,* Vol-116, pp. 163-170, 1994.

Pucha R. V, Pyland J and Sitaraman. S. K., "Damage Metric-Based Mapping Approaches for Developing Accelerated Thermal Cycling Guidelines for Electronic Packages", *International Journal of Damage Mechanics,* Vol 10, No. 3 (2001), pp. 214-234

Pyland, J., 2002, "Damage Metric-Based Thermal Cycling Guidelines for Area-Array Packages used in Harsh Thermal Conditions.

Schubert, A., Dudek, R., Auersperg, J., Vogel, D., Michel, B., Reichl, H., Suhir, E., Shiratori, M., Lee, Y.C., Subbarayan, G. 1997, "Thermo-mechanical Reliability Analysis of Flip-Chip Assemblies by Combined Microdac and Finite Element Method", *Proceedings of the Pacific Rim/ASME International Intersociety Electronic and Photonic Packaging Conference. INTERpack '97*, ASME, Kohala Coast, HI, EEP-Vol. 19-2, pp. 1647-1654.

Shi, X. Q., Pang, H. L. J., Zhou, W., and Wang, Z. P., 1999, "A Modified Energy-Based Low Cycle Fatigue Model For Eutectic Solder Alloy", *Scripta Materialia,* Vol. 41, No-3, pp. 289-296, 1999

Shi, X. Q., Pang, H. L. J., Zhou, W., and Wang, Z. P., "Low Cycle Fatigue Analysis of Temperature and Frequency Effects in Eutectic Solder Alloy", *International Journal of Fatigue,* Vol 22, pp. 217-228, 2000.

Shine, M. C., and Fox, L. R. 1987, "Fatigue of Solder Joints in Surface Mount Devices", Low Cycle Fatigue- *Low Cycle Fatigue-ASTM Special Technical Publication 942*, ASTM, Philadelphia, PA, pp. 588-610.

SRC/CINDAS Microelectronics Packaging Materials Database, Sept. 1995 release

SRC/CINDAS Microelectronics packaging Materials Database, Version 2.21, 1999 release

Syed, A and Doty. M., "Are We Over Designing for Solder Joint Reliability? Field vs. Accelerated Conditions, Realistic vs. Specified Requirements", *Proc 49th Electronic Components and Technology Conf*, 1999, pp.111-117.

Tummala, R., Rymaszewski E. J., Klopfenstien, A. G., (eds) 1997, *Microelectronics Packaging Handbook*, 2nd Edition, Chapman and Hall, New York

Tunga, K., Pyland, J., Pucha, V. R., and Sitaraman, S. K., "Study on the Choice of Constitutive and Fatigue Models in Solder Joint Life Prediction", *ASME Proceedings of IMECE 2002,* New Orleans, Nov-2002.

Wang, G. Z., Cheng, Z. N., Becker, K., and Wilde, J, "Appling Anand Model to Represent the Viscoplastic Deformation Behavior of Solder Alloys", *Journal of Electronic Packaging,* Vol. 123, pp. 247-253, Sept 2001.